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IMPLEMENTING HAMMING CODES TO THE CACHE LEVEL OF A MEMORY HIERARCHY

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Abstract. In this paper we will apply a Hamming code to the cache level of a memory hierarchy. From the category of SEC-DED (Single Error Correction Double Error Detection) codes we select the Hamming code. For correction of single-bit error we use a syndrome decoder, a syndrome generator and the check bits generator circuit We have implemented the Hamming (21,16,5) code, to the cache Tag memory and we have determined data overhead and overhead induced by the supplementary circuits for the error correction

Keywords: Hamming code, cache Tag, cache RAM.