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VLSI IMPLEMENTATION OF CMOS LOW POWER FULLY DIFFERENTIAL PHASE-LOCKED LOOP

BY

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Abstract. High-speed low-power phase-locked loop (PLL) circuits find wide application in high-performance communication systems. This paper describes the VLSI implementation of a CMOS low power fully differential PLL circuit. The phase detector of the proposed PLL is represented by an analog multiplier implemented with a Gilbert cell and the voltage controlled oscillator is configured as a ring oscillator with two stages which provide quadrature outputs; it incorporates phase shift elements to obtain a wider tuning range. The frequency operation range is situated between 40…740 MHz and can be set by using digital command logic. The circuit provides an output signal having THD ≤ 1% over all this range and can lock to the input in the presence of temperature, supply voltage and process variations. The current consumption of the circuit is 2.7 mA from a 3.3 V supply voltage. The simulations performed in a 0.18 μm CMOS technology confirm the theoretical results.

Key words: PLL; Gilbert cell; transconductance; VCO; ring oscillator; LPF; CMOS; VLSI.