BULETINUL INSTITUTULUI POLITEHNIC DIN IAŞI
Publicat de
Universitatea Tehnică „Gheorghe Asachi” din Iaşi
Tomul LVII (LXI), Fasc. 2, 2011
Secţia
ELECTROTEHNICĂ. ENERGETICĂ. ELECTRONICĂ

AN INTEGRATED VOLTAGE CONTROLLED CURRENT SCALOR

BY

MANUELA MOCANU[1,*], RĂZVAN VIERU[1], ARCADIE CRACAN[1], PAVEL-VIOREL BRÎNZOI[1] and LIVIU GORAŞ[1,2]

[1]“Gheorghe Asachi” Technical University of Iaşi
Faculty of Electronics, Telecommunications and Information Technology,
[2]Romanian Academy, Iaşi Branch
Institute of Computer Science

Received: November 5, 2010
Accepted for publication: March 12, 2011

Abstract. An integrated voltage controlled current scalor is presented. The circuit, based on a current amplifier with voltage controlled amplification, was designed in a 0.35 um AMS technology. A theoretical analysis and simulation results for several linear and nonlinear impedances are given.

Key words: *x*-controlled current scalor; impedance scaling; variable gain current amplifier.

1. Introduction

The *x*-controlled current scalor, where *x* can be a voltage or a current, has been introduced by Goraş (1979) as a particular case of the *x*-controlled power scalor.

The linear *x*-controlled power scalor (LXCPS) has been defined as a nonlinear four-port characterized by the following transmission matrix between ports 1 and 2:

[*] Corresponding author: *e-mail*: mmocanu@etti.tuiasi.ro

$$T_{1-2(L)}^{P}=\begin{bmatrix} K_v x & 0 \\ 0 & K_i x' \end{bmatrix}, \tag{1}$$

where x and x' can be currents or voltages applied at the remaining ports.

The linear x-controlled voltage scalor (LXCVS) and the linear x-controlled current scalor (LXCCS) are nonlinear three ports characterized, respectively, by the transmission matrices between ports 1 and 2

$$T_{1-2(L)}^{V}=\begin{bmatrix} K_v x & 0 \\ 0 & 1 \end{bmatrix},\quad T_{1-2(L)}^{V}=\begin{bmatrix} 1 & 0 \\ 0 & K_i x' \end{bmatrix}, \tag{2}$$

the controlling variables x and x' being applied at the third port.

The impedance $Z_1(s)$ "seen" at port 1 of an LXCPS loaded at port 2 with $Z_2(s)$ is

$$Z_1(s)=\frac{K_v x Z_2(s)}{K_i x'}. \tag{3}$$

Making use of the loop or cut-set equations it is easy to prove the following

T h e o r e m 1. *An LXCPS loaded at port 2 (1) with an arbitrary linear one-port, behaves at port 1 (2) like the initial one-port having the resistances, inductances, and elastances multiplied by* $K_v x / K_i x'$ ($K_i x' / K_v x$).

If controlled sources or coupled inductors are present, the theorem is valid according to the dimension of the parameters; dimensionless parameters do not change.Invoking piece-wise linearization, the above theorem can be extended to nonlinear networks.

T h e o r e m 2. *An LXCPS loaded at port 2* (*1*) *with an arbitrary nonlinear one-port, behaves at port 1* (*2*) *like the initial one-port having the elements characteristics scaled by* $K_v x$ ($1/K_v x$) *on the v- and* Φ*-axis and by* $K_i x'$ ($1/K_i x'$) *on the i- and q-axis.*

If x is a voltage, the above scalors are obviously voltage controlled. Moreover the voltage controlled current scalor can be considered as a circuit dual of that exhibiting the well-known Miller effect and having as ingredient the presence of a double controlled current source. In a previous work of one of the authors (Goraş, 1979) two implementations with discrete components of the LXCVS and LXCCS are reported. The aim of this paper is to present an integrable version of a voltage controlled current scalor based on a variable gain current amplifier designed in a CMOS technology.

2. Principle of Operation

The proposed structure implements in CMOS technology the schematic shown in Fig. 1. Unlike the solution proposed by Goraş (1979) in this one the

unity term that appears in the denominator has not been absorbed in the controlling factor. Besides, the control voltage is not necessary linear.

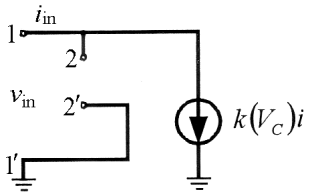

Fig. 1 – Ideal representation of the proposed structure.

From elementary considerations, the impedance "seen" at port 1-1′ while port 2-2′ is loaded with a linear impedance $Z(s)$ is

$$Z_{in}(s) = \frac{Z(s)}{1 + k(V_C)}. \tag{4}$$

From the above equation it is clear that the impedance $Z(s)$ can be scaled by means of the current gain, k, which will depend on a control voltage, V_C . Both negative and positive scaled impedances can be obtained depending on the sign of $1 + k(V_C)$.

The simplified structure of the proposed current controlled impedance is shown in Fig. 2, being based on a series-shunt feedback amplifier (Sansen, 2006).

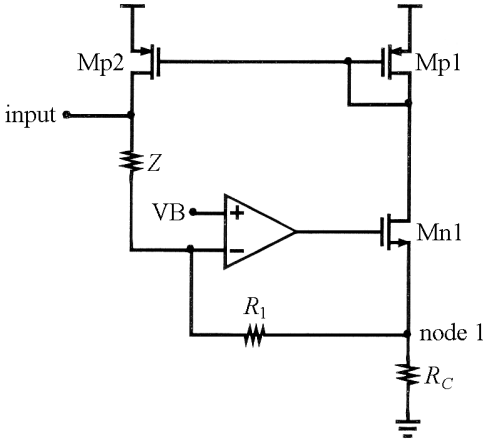

Fig. 2 – Simplified structure of the voltage controlled impedance.

The structure consists of a current amplifier working with an operational amplifier implemented as a simple one-stage NMOS differential amplifier and two resistances, R_1 and R_C , the latter being that which will

provide the control of the gain factor. Other ways of obtaining continuous gain adjustment in current amplifiers are reported in some works (Koli, 2000; Toumazou *et al.*, 1990). For identical geometry of the CMOS transistors, the current gain is given by

$$k = 1 + \frac{R_1}{R_C}. \tag{5}$$

The advantages of the proposed schematic are that the current gain depends only on a resistors ratio and the input impedance is very low, ideally zero. This represents an advantage in comparison with the structure reported by Aguado Ruiz *et al.* (2011).The current flowing through the impedance $Z(s)$ we intend to scale, is k times amplified by the current amplifier, copied by the simple PMOS current mirror and injected into the input node. The main problem that appears when the resistor value, R_C, is changed is that it influences the DC potential of the source of transistor Mn1. The solution adopted in this work keeps the DC potential at node 1 constant preventing the operating point of transistor Mn1 from changing, when modifying the value of R_C . The proposed solution is to use an additional current source implemented by transistor M5, as shown in Fig. 3. By choosing an appropriate value for its gate source voltage, we keep the M0 NMOS transistor implementing the R_C resistance in deep triode region. Therefore transistor M0 behaves as a variable resistance, whose value is given by

$$r_{ds} = \frac{1}{m_n C_{ox}(W/L)(V_{GS} - V_{TH})}, \tag{6}$$

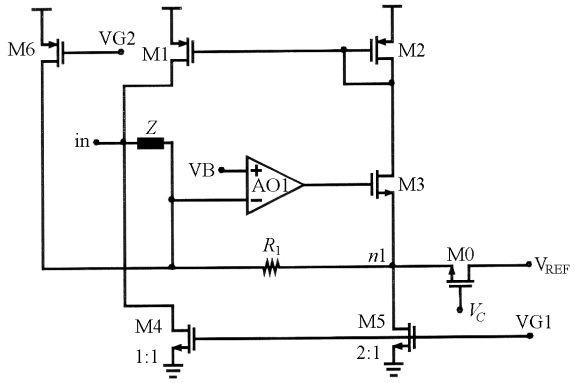

Fig. 3 – The proposed current controlled impedance.

where μ_n represents the NMOS transistor mobility, C_{ox} – the transistor gate capacitance and W / L – the transistor aspect ratio.

From (6) it can be concluded that a way of changing its equivalent resistance is to modify its gate source potential. In order to obtain a linear current gain we must ensure that both R_1 and R_C are linear. R_1 is implemented using a 0.35 um AMS technology rpolyh resistance whose value is 30 kΩ, while R_C is implemented using an NMOS transistor. For its equivalent resistance to be linear, we must ensure that it operates in deep triode region (Johns & Martin, 1997). Therefore, the following condition must be satisfied:

$$V_{DS} \ll 2(V_{GS} - V_{TH}), \tag{7}$$

where V_{DS} represents the transistor drain source voltage, V_{GS} – the transistor gate source voltage and V_{TH} – the transistor threshold voltage. In the following a mechanism that keeps the drain source voltage of the transistor implementing R_C very small is presented. It is based on choosing an appropriate value for the gate-source voltage of transistor M5 so that its drain source voltage equals V_{REF}. Acting in this manner, the drain source voltage of M0 transistor working as a variable resistance is theoretically zero ensuring its operation in deep triode region. As a consequence, the DC potential at node $n1$ remains unchanged, being equal to V_{REF} regardless of the variations of the gate potential of the transistor implementing R_C . The current gain amplifier is thus affected in a linear way by keeping the NMOS transistor implementing R_C in deep triode region. Imposing the potential at node $n1$ equal to V_{REF}, the necessary voltage V_{G1} to be applied at the gate of transistor M5 is given by

$$V_{G1} = V_{TH} + \sqrt{\frac{4(V_B - V_{REF})/R_1}{m_n C_{ox}(W/L)(1+lV_{REF})}}, \tag{8}$$

where λ represents the channel length modulation coefficient.

By replacing Z, in Fig. 3, with a resistance, a capacitance, or a diode, we obtain a scaled resistor, a scaled capacitance or a scaled diode, respectively.

3. Simulation Results

The structure was implemented in a 0.35 um AMS technology provided by AUSTRIA MICROSYSTEMS. The program used for performing the simulation was Mentor Graphics. The performances of the simple one-stage operational amplifier are summarized in Table 1.

We keep the R_1 value fixed while changing the value of R_C . R_C is modified by changing the gate potential, V_C , of the NMOS deep triode region, M0. For V_C varying between 1.5 V and 3.3 V the R_C resistance and current gain k values are given in Table 2.

Table 1
Performances of the Simple Differential Amplifier

Gain dB	Bandwidth KHz	Unity gain bandwidth MHz	Phase margin degrees
52	745	158.08	70

Table 2
R_C and k Values for Different V_C Voltages

V_C, [V]	R_C, [kΩ]	k
1.5	3.86	8.77
2.3	1.06	29.3
3.3	0.8	38.5

First, the impedance to be scaled, *Z*, has been replaced with a 1 kΩ resistance.

The equivalent resistance seen at the input node, v_{IN}, is given by

$$R_{EQU} = \frac{R}{1+k(V_C)}. \tag{9}$$

The resulting DC characteristics are shown in Fig. 4 for three different values of V_C voltage. The simulated equivalent resistance values as well as the calculated ones are given in Table 3.

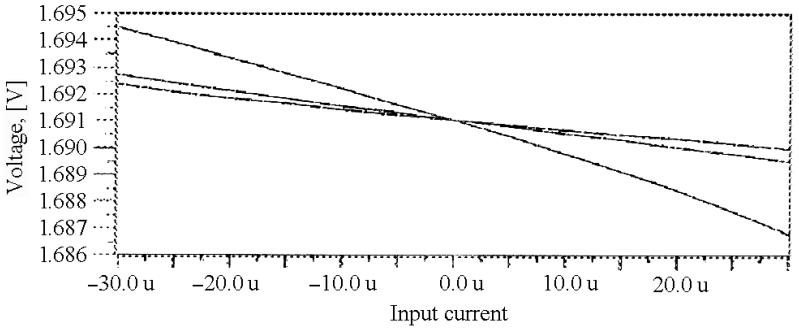

Fig. 4 – DC characteristics of the scaled resistance.

Table 3
Simulated and Calculated R_{EQU} Values for Different V_C Voltages

V_C, [V]	Simulated R_{EQU} values, [kΩ]	Calculated R_{EQU} values, [kΩ]
1.5	0.17	0.2
2.3	0.033	0.039
3.3	0.024	0.028

A periodic steady-state analysis was performed using a sinusoidal current source at the input node, in order to measure the total harmonic distortion (THD) of the circuit. The simulation results, for different input

current signal amplitudes varying from 1 uA to 5 uA, are shown in Fig. 5. Three different values for V_C voltage source have been considered: V_C = 1.5 V, V_C = 2.3 V, V_C = 3.3 V.

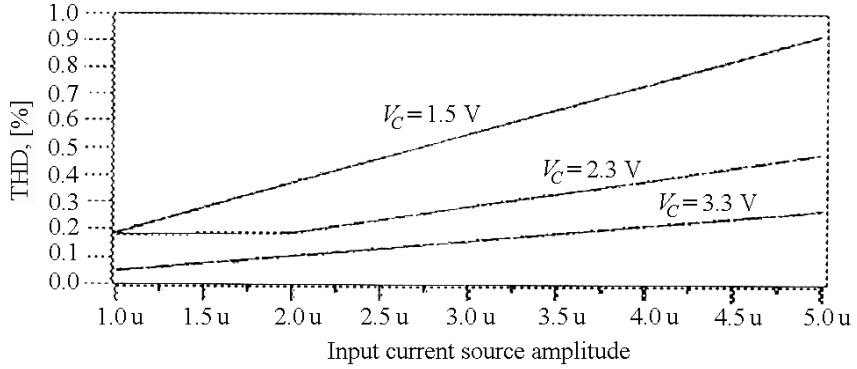

Fig. 5 – Total Harmonic Distorsion Coefficient.

Next we replace the impedance *Z* with a PMOS transistor in diode configuration. The static characteristics of the diode current as a function of the voltage across it are shown in Fig.6.

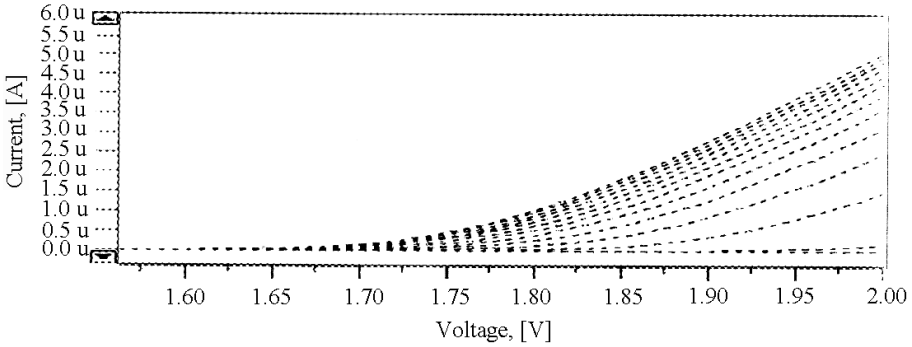

Fig. 6 – Static characteristics of the diode-connected transistor.

The equation describing the scaling of the PMOS diode connected current–voltage characteristics is

$$i=(1+k)I_{SS}\left[\mathrm{e}^{(V_{IN}-V_B)/V_T}-1\right], \tag{10}$$

where: *i* represents the current flowing through diode connected transistor, I_{SS} – the diode saturation current, V_{IN} – the input voltage source used to determine the static current–voltage characteristics, V_B – the DC voltage source applied at the positive input terminal of the AO implementing the current amplifier and V_T – the thermal voltage.

Last, we replace Z with a 1 pF capacitor C. The equivalent capacitance seen at node v_{IN} is given by

$$C_{EQU} = (1+k)C. \tag{11}$$

The AC plots showing the magnitude and phase of the equivalent input capacitance are shown in Fig. 7 for different V_C voltage source values. The simulated equivalent capacitance values as well as the calculated ones are given in Table 4.

Table 4
Simulated and Calculated C_{EQU} Values for Different V_C Voltages

V_C, [V]	Simulated C_{EQU} values, [pF]	Calculated C_{EQU} values, [pF]
1.5	12.8	9.77
2.3	33.5	30.3
3.3	44.1	39.5

The difference between the simulated and calculated equivalent input capacitance is a consequence to the fact that the actual value of the capacitance C we want to scale is 1 pF plus the value of the parasitic capacitances at the node v_{IN}.

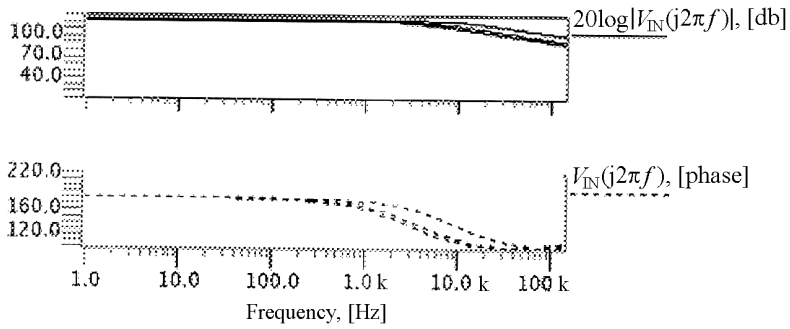

Fig. 7 – Magnitude and phase of the equivalent input capacitance.

4. Conclusions

In this work, an integrated voltage controlled current scalor is presented. The circuit is based on a current amplifier with voltage controlled amplification. A solution is proposed that prevents the circuit's DC operating points from changing, while continuously varying the current gain. Several linear and nonlinear elements are scaled in order to show the circuit principle of operation.

Acknowledgment. This paper was realized with the support of EURODOC and BRAIN "Doctoral Scholarships for Research Performance at European Level" project, financed by the European Social Found and the Romanian Government.

REFERENCES

Aguado Ruiz J., Lopez-Martin A.J., Ramirez-Angulo J., *Three Novel Improved CMOS Capacitance Scaling Schemes*. Internat. J. of Circ. Theory a. Appl., January 2011 (on line).

Goraş L., *The x-Controlled Scalor and Its Application to Network Synthesis*. IEEE Trans. on Circ. a. Syst., **CAS-26**, *4*, 288-290 (1979).

Johns D., Martin K., *Analog Integrated Circuit Design*. J. Wiley, NY, 1997.

Koli K., *CMOS Current Amplifiers*: *Speed versus Nonlinearity*. PH. D. Diss., Helsinki Univ. of Technol., Finland, 2000.

Sansen W.M.C., A*nalog Design Essential*. Ch. **14**, *Feedback Transimpedance and Current Amplifiers*. Springer, Dordrecht, 2006.

Toumazou C., Lidgey F.J., Haigh D., *Analogue IC Design*: *The Current Mode Approach*. Peter Peregrinus, London, 1990.

SCALOR DE CURENT CONTROLAT ÎN TENSIUNE

(Rezumat)

Se prezintă un scalor de curent controlat în tensiune. Circuitul se bazează pe un amplificator de curent cu amplificare controlată în tensiune şi este realizat într-o tehnologie de 0.35 um. Sunt date rezultate teoretic şi simulări pentru a evidenţia principiul de funcţionare al circuitului.