A NOVEL SCHMITT TRIGGER AND ITS APPLICATION IN OSCILLATION BASED BIST

BY

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Abstract. A novel structure for a Schmitt trigger is presented. The novelty relies in the fact that it has an atypical form of hysteresis and so it is suitable for use in a classical Oscillation Based Test (OBT) method where a special characteristic for the Schmitt-trigger is needed. The present work is a continuation of a previous OBT study. The circuit is discussed in the context of the OBT method and implemented in a standard CMOS 0.35 μm process.

Key words: oscillation based test; BIST; Schmitt trigger; circuit, testing.

1. Introduction

An analytical method to determine the response of a certain class of circuits that are built for second-order filters was presented in a previous paper (Cojan *et al.*, 2010). The Oscillation Based Test (OBT) method allows the designers to test on-chip the proper operation of a filter by evaluating the selected oscillation parameters when it is closed in a feedback loop with a non-linear element. We showed that in certain cases, namely for a second order system with real poles, the common setup for the oscillation based test fails to oscillate. To circumvent this inconvenient we proposed a novel circuit structure that makes use of a novel Schmitt trigger.

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The Schmitt trigger is widely used in the analog and digital domain of integrated circuits. It is a viable alternative to a standard comparator because of its versatility due to the hysteresis. Numerous uses of the Schmitt trigger can be found: high density memory circuits (Ochii *et al.*, 1989), low THD amplifiers (Chun Kit Lam *et al.*, 2009), low-voltage devices that can accept a high-voltage input (Shih-Lun Chen *et al.*, 2005) or signal restoration (Secarcanu *et al.*, 1999). Its hysteresis depends on various factors, mainly process parameters, and so extensive work can be found to alleviate this (Di Cataldo *et al.*, 1992).

A typical OBT circuit is shown in Fig. 1 *a*. The using idea behind a feedback configuration method is to use a supplementary block that will enable oscillations using the filter in the test mode, a consequence of the natural oscillation potential exposed by filters. The feedback loop can be positive or negative. In the case of a mild non-linearity added around the filter, Barkhausen conditions can be used to determine the gain and phase necessary to build oscillations. In the case of a discontinuous non-linearity Barkhausen conditions cannot be applied as the system cannot be linearized.
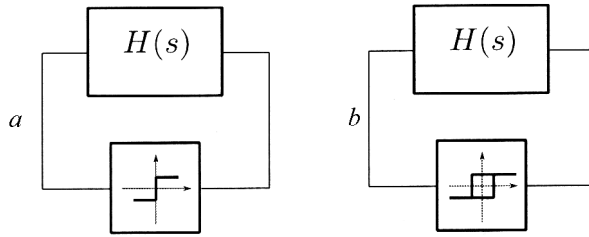

Fig. 1 – *a* – Typical OBT circuit; *b* – used OBT setup.

In the previous mentioned paper (Cojan *et al.*, 2010) the Weidelich method is used to obtain the semi-periodical component of the response of a linear, time-invariant (LTI) system, to a semi-periodical excitation in the given context of the OBT configuration that has a comparator as the non-linear element. It has been shown in the below mentioned paper that the generating signal of the periodic steady state filter output in time domain has the response of the form

$$y_g(t) = \frac{2IV_{\text{ref}}}{p_b - p_a} \left[\frac{1 - e^{-p_a(T-q)}}{1 - e^{-p_aT}} s(t)e^{-p_at} - \frac{1 - e^{-p_b(T-q)}}{1 - e^{-p_bT}} s(t)e^{-p_bt} - s(t-q) \times \right.$$

$$\left. \times \left(e^{-p_a(t-q)} - e^{-p_b(t-q)} \right) + s(t-T) \left(\frac{e^{-p_a(T-q)} - e^{-p_aT}}{1 - e^{-p_aT}} e^{-p_a(t-T)} - \frac{e^{-p_b(T-q)} - e^{-p_bT}}{1 - e^{-p_bT}} e^{-p_b(t-T)} \right) \right]. \quad (1)$$

The comparator output transition moments in closed loop are determined from the zero-crossing conditions $\lim_{t \to q} y_G(t) = 0$ and $\lim_{t \to T} y_G(t) = 0$ of the

filter output signal found in (1). In the case of a second order real poles system it has been shown in the cited previous paper that the equations system yielded by these conditions has no real solutions, therefore the circuit fails to oscillate.

Obviously the usual OBT setup cannot be applied here because the filter's output signal never crosses zero. We propose a new OBT setup as seen in Fig. 1 *b* for which the comparator is replaced with a Schmitt trigger such that the output transition moments are determined in this case by the threshold crossing condition $\lim_{t \to q} y_G(t) = V_{th,h \to l}$ and $\lim_{t \to T} y_G(t) = V_{th,l \to h}$. The equations written for the new setup, which account for the thresholds, are transcendent and therefore only numerical solvers apply.

A typical response of such an arrangement for the case of an ideal comparator using numerical solvers is given in Fig. 2. The comparator's thresholds have been set to ±0.5 V.
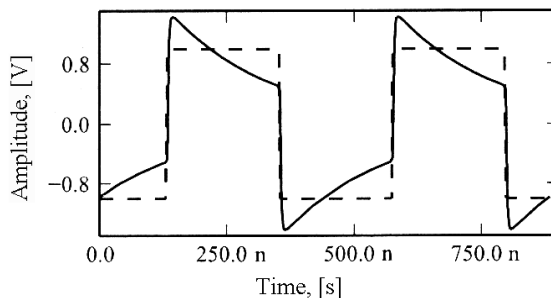

Fig. 2 – The comparator response (dashed)
and the filter response (continuous) for real poles.

It has been shown, in the mentioned previous paper, that large variations in the pole position determine a large variation in the oscillation period in the case of an OBT using a dual threshold Schmitt trigger. The proposed method, a variation of the classical OBT, allows variations in the non-dominant pole position to be detected. The Schmitt trigger is actually an application of a comparator that does not switch the output until the input changes sufficiently to trigger a change. A comparator can have: inverting and non-inverting configurations. The main difference between a usual comparator and a Schmitt trigger is that the trigger presents two transitions trajectories, one for the low to high transition and another for the high to low transition, making it behave as a circuit with memory. The usual transfer characteristic of a typical non-inverting Schmitt trigger comparator is given in Fig. 3 *a*. It does not describe the needed characteristic from Fig. 2 because when the input is higher than a certain chosen threshold, the output is high, when the input is below a different lower chosen threshold, the output is low, and when the input is between the two thresholds the output retains its value. We can observe that in

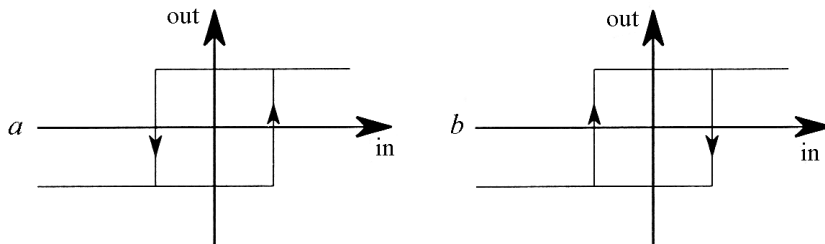this case the input must drop significantly below the lower threshold so that the output switches its value.

Fig. 3 – Standard (*a*) and proposed (*b*) Schmitt trigger characteristics.

The transfer characteristic of the proposed Schmitt trigger is presented in Fig. 3 *b* and it can be observed that the output changes its state according to the thresholds and the slope of the signal. In the following we present the implementation of the proposed Schmitt trigger, the necessity of which has been suggested in the above paper (Cojan *et al.*, 2010).

The proposed circuit is presented in Fig. 4. It consists of a novel slope detector followed by the selector that selects between the two threshold voltages based on the input signal slope.
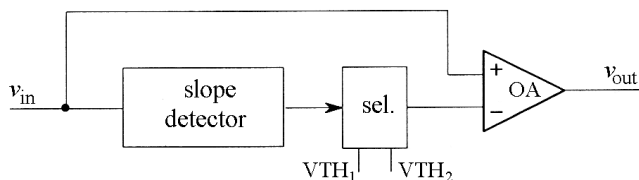

Fig. 4 – Simplified schematic of the proposed Schmitt trigger.

The circuit will thus detect the slope of the input signal, and enables a certain threshold voltage through the selector. To obtain the usual Schmitt trigger characteristic one can insert an inverter between the selector and the slope detector. After that, the input signal is compared with the selected threshold voltage through a standard operational amplifier configured as a comparator. For this solution the input signal must not change its slope before the next threshold, this behavior being due to the use of a slope detector. These signals are specific to the considered filter.

2. Proposed Slope Detector

The simplified schematic of the slope detector is represented in Fig. 5.

The circuit detects the slope of the applied signal at the input by converting the charging/discharging currents of the capacitor into two voltages,

v_{OUT1} and v_{OUT2}, that appear across the resistances R_1 and R_2. The negative feedback loop will set the DC voltage at the capacitor node at the desired input DC voltage. For a rising signal at the input, the transistor M_1 enters conduction and charges the capacitor C from V_{DD}. The transistor M_2 is off so all the current from V_{DD} is entering C through M_1. For the decreasing part of the input signal, the capacitor will discharge through M_2 to GND, M_1 being off. So the current through R_1 and R_2 will reflect the slope of the input signal.
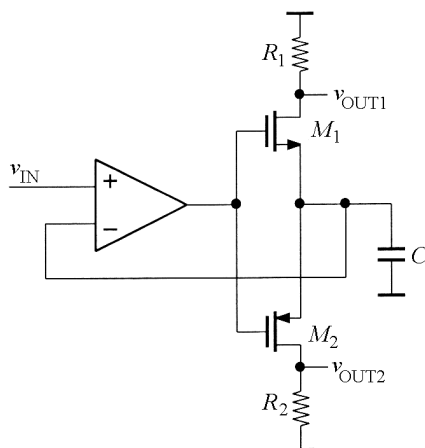

Fig. 5 – Proposed slope detector.

Due to the dead zone of the class B output stage the slope detector will exhibit a delay between the moment when the input signal's derivative changes the sign and the moment the output switches it's state. Considering that transistors M_1 and M_2 are cut off for $v_{\text{GS}} \le V_{\text{TH}}$ and that the operational amplifier, OA, has finite gain, a, the total delay introduced by the slope detector can be determined as following. Considering $v_{\text{ind }z}$ the value of the input signal that drives the slope detector into its dead zone, the time delay, t_{dz}, of the circuit response depends on the threshold voltages of *nmos* transistor M_1 and *pmos* transistor M_2, and on the gain of the OA. Thus t_{dz} can be determined from relation

$$v_{\text{ind }z} = \frac{\left|V_{\text{TH}p}\right| + V_{\text{TH}n}}{a}. \tag{2}$$

In the case of a harmonic signal at the input with an amplitude equal to $v_{\text{IN}} = V_{\text{IN}}\cos \omega t$, that has a DC component, V_{DC}, the value of the time delay, t_{dz}, can be determined from equation

$$\left(V_{\text{DC}} + V_{\text{IN}}\right) - \left(V_{\text{DC}} + V_{\text{IN}} \cos wt\right) = \frac{\left|V_{\text{TH}p}\right| + V_{\text{TH}n}}{a} \tag{3}$$

obtained from (2) and consequently

$$2V_{\text{IN}} \sin^2 \frac{wt_{dz}}{2} = \frac{\left|V_{\text{TH}p}\right| + V_{\text{TH}n}}{a} . \tag{4}$$

Using the approximation $\sin x \cong x$ for $x \to 0$ and considering that $t_{dz} \ll T$, where T is the input signal period, eq. (4) becomes

$$V_{\text{IN}} \frac{\left(wt_{dz}\right)^2}{2} = \frac{\left|V_{\text{TH}p}\right| + V_{\text{TH}n}}{a}$$

and from here it results

$$t_{dz} = \frac{1}{w} \sqrt{\frac{2}{a} \cdot \frac{\left|V_{\text{TH}p}\right| + V_{\text{TH}n}}{V_{\text{IN}}}} . \tag{5}$$

The final solution for t_{dz} is

$$\frac{t_{dz}}{T} = d_{dz} = \frac{1}{2p} \sqrt{\frac{2}{a} \cdot \frac{\left|V_{\text{TH}p}\right| + V_{\text{TH}n}}{V_{\text{IN}}}} . \tag{6}$$

Eq. (6) shows that for a precise detection of the switching moment of the slope of the input signal, the value of t_{dz} / T ratio must be as small as possible and this further asks that the gain of the OA be as large as possible. In the implemented example, knowing that $|V_{\text{TH}p}| = 650$ mV, $V_{\text{TH}n} \cong 550$ mV, $V_{\text{IN}} = 300$ mV and $a = 50$, eq. (6) yields a theoretical value of $t_{dz} / T = 0.063$. Furthermore relation (6) shows if a smaller error is desired, by example 1% instead of 6.3%, in the same conditions an OA with a gain of $a = 16,000$ which is extremely difficult for high frequencies.

In previous calculations the finite output resistance of the circuit that charges and discharges the capacitor C has been neglected. The moment when the output resistance of the output circuit has a large value, is the one in which $M_1(M_2)$ are starting to work. Even if the stage consisting of M_1 and M_2 is in the negative feedback loop, that determines the drop of the output resistor of the stage, the delay time of the response will be larger than the previously estimated t_{dz} by eq. (6).

The performance of the presented circuit depends on many factors. One of them is the size of the capacitor. If the capacitor is too small the circuit will not respond properly; if it is too large it will not be quickly charged and erroneous output signals will be obtained. The value of capacitor C is chosen so that the supplementary errors introduced by the final circuit represented in Fig.

7, namely the current mirror clients M_5 and M_6 , are kept at a minimum. For an ideal OA we can write

$$i_c = C\frac{dv_{IN}}{dt} \tag{7}$$

and considering that $v_{IN} = V_{IN}\cos wt$ we obtain

$$i_c = CwV_{IN}\cos wt \tag{8}$$

and because $\cos wt \leq 1$ it results that

$$i_c \leq CwV_{IN} , \tag{9}$$

that represents the main condition for choosing the value of capacitor C.

In Fig. 6 is represented the current from the capacitor C overlapped with the derivative of the input signal multiplied by the capacitor value that would be the response in the case of an ideal amplifier. It can be observed that aside from the moments when the input signal forces the circuit in the dead zone the responses are aligned, which denotes the fact that the effect of the finite output resistance can be neglected.
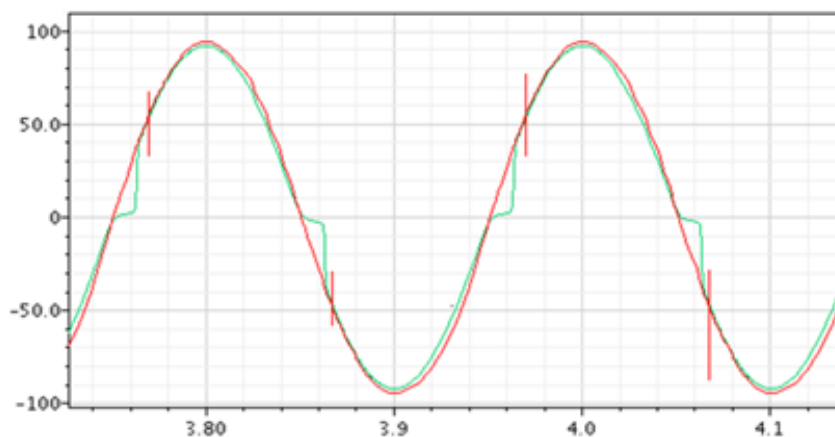

Fig. 6 – Current from *C* *versus* the ideal derivative of the input
signal multiplied by the value of the capacitor *C*.

The currents for the slope input variations can be easily acquired for further manipulation with two current sources implemented with MOS transistor. The final circuit implementation is represented in Fig. 7, where the drains of the transistors M_5 and M_6 are connected together, so that the effect of

the capacitor is increased and thus more easily observable as a voltage at the output.
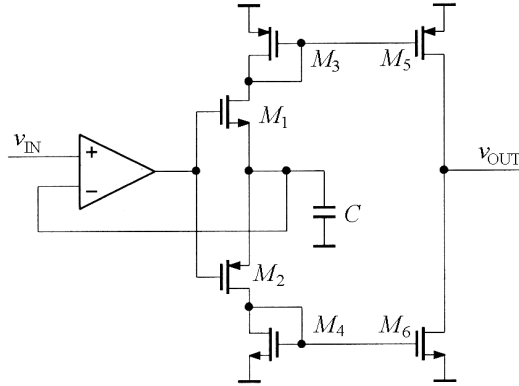

Fig. 7 – The final slope detector.

For simulations, a 10 MHz signal has been applied at the input. A 10 pF capacitor has been chosen, *nmos* transistor M_1 have a W/L ratio of 5 u/350 n and *pmos* M_2 transistors, 10 u/350 n. The DC value at the circuit input has the value of 900 mV and thus the negative feedback loop is forcing a DC value at the capacitor node of 893 mV for an OTA with $a \approx 50$, that being easily implementable.

Simulations of the circuit represented in Fig. 7 in the time domain are found in Fig. 8.
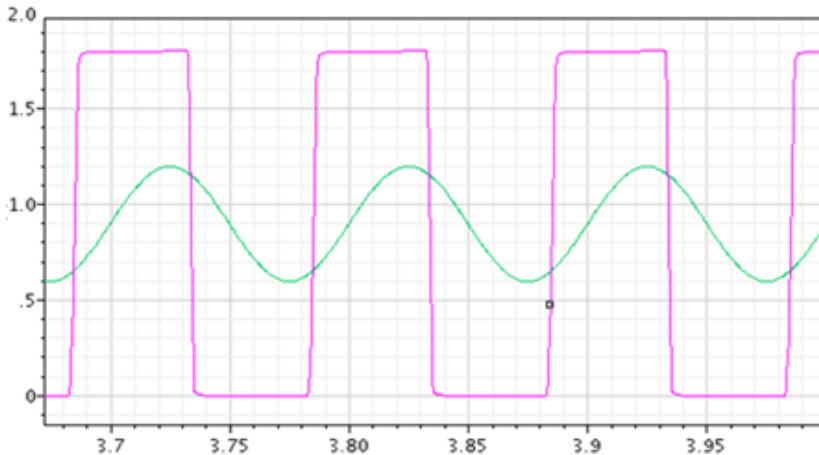

Fig. 8 – Response of the proposed slope detector.

We can observe that when the signal is rising, the output of the slope detector has the logical value of "1" and while the signal is decreasing the output has the "0" logical value. In Fig. 8 signals for a 5 MHz input are

presented. The measured error between the input and the slope detector response is 6.3% of the input signal period.

3. The Final Circuit

The operational amplifier from Fig. 4 is a simple structure with respect to the frequency behavior because the entire system is basically frequency limited by it. The proposed OA is represented in Fig. 9.
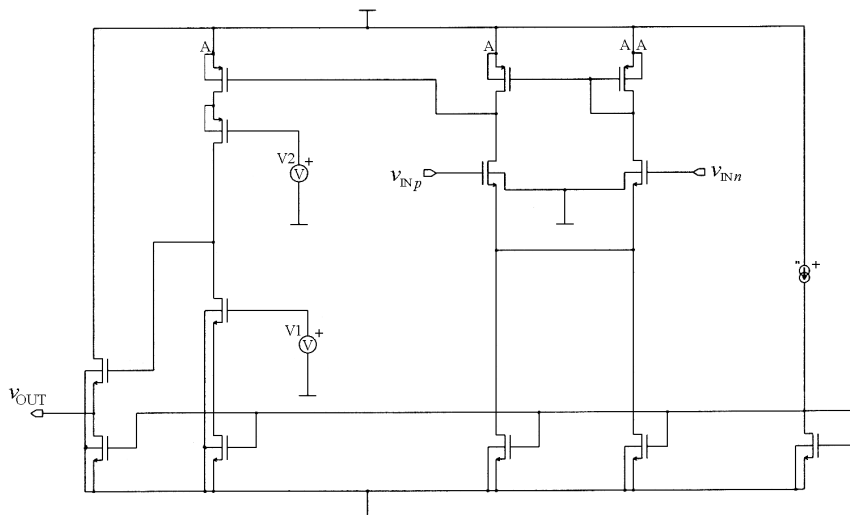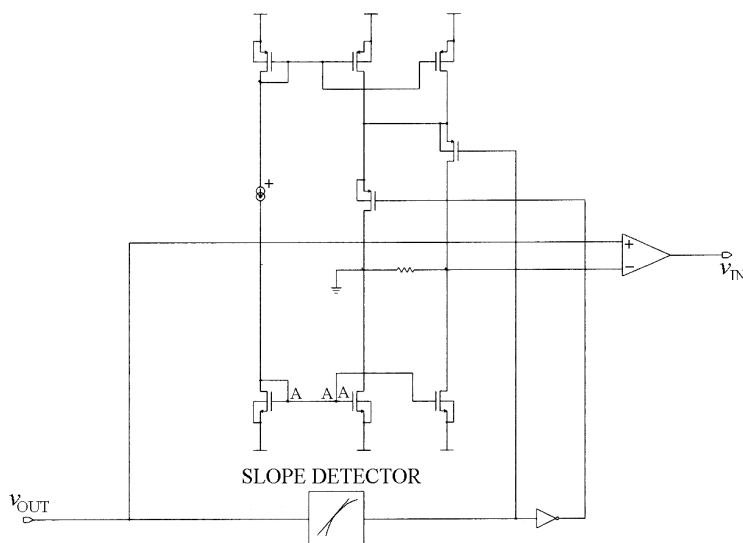

Fig. 9 – Implemented OA.

Fig. 10 – Final schematic of the proposed Schmitt trigger.

The used OA presents a simple differential pair input and a repeater stage at the output. Its frequency behavior is especially important and we must ensure that a certain minimum gain is satisfied for a maximum desired frequency.

The final Schmitt trigger is represented in Fig. 10. It consists of the slope detector that drives the circuit to select one of the thresholds, depending on the slope of the input signal and a comparator. The two thresholds are generated across the resistor in the inverting input of the OA by means of current switching through two current sources that are driven by the output signal from the slope detector and its inverted value. The thresholds can be modified by the current at the current sources head and the value of the resistor. The final comparator is the OA represented in Fig. 9. The transfer characteristic for the Schmitt trigger represented in Fig. 11 has been obtained from low frequency transient simulation.
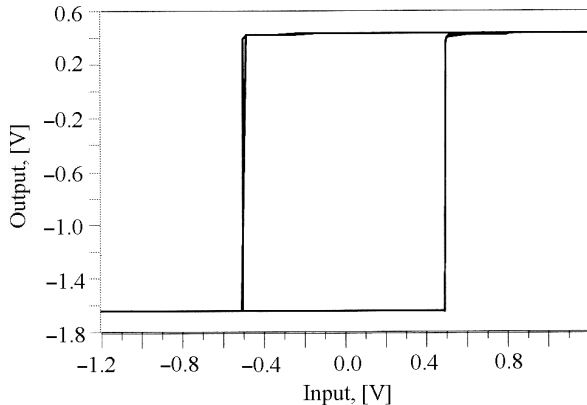

Fig. 11 – Schmitt trigger transfer characteristic.

Simulations present the input signal and the output final Schmitt trigger response. It is noticeable that the output signal starts to switch when the thresholds are detected. The delay appears due to the limited gain of the final OA and due to the finite output resistance of the charge/discharge circuit of capacitor C and of the finite response time of the current sources implemented with M_3, M_4 and M_5, M_6.

4. OBT Results

Simulation results of a parametric analysis of the complete OBT circuit shown in Fig. 1 *b* are presented. The proposed Schmitt trigger is implemented at transistor level as it is described in the previous sections. The filter is implemented in VerilogA. Simulations are presented for threshold variations from ±0.1 V to ±0.8 V in 8 steps. Filter and comparator outputs are presented in Fig. 12.

The filter used in this example has the dominant pole at 100 kHz and the non-dominant pole at 1 MHz. We can observe that the position of the second pole has its impact on the oscillation frequency as it was explained previously (Cojan, 2010).
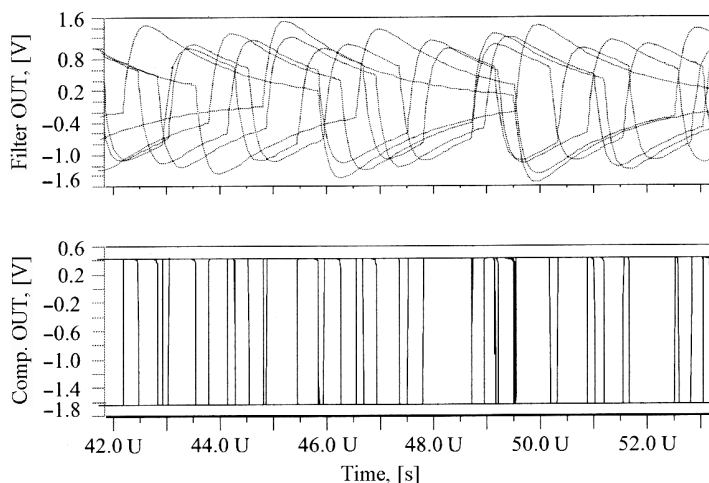
Fig. 12 – Filter and comparator outputs from OBT circuit.

5. Conclusions

A novel Schmitt trigger circuit is proposed. The circuit is based on a slope detector that uses an amplifier and a class B output stage to charge and discharge a capacitor. It is suitable for a modification of the classical OBT method reported in a previous work (Cojan, 2010), where an atypical Schmitt trigger is needed for BIST circuitry. It can easily be designed to work for high frequency. The circuit can use small capacitor values even at low frequencies, which represents an advantage in respect to circuit area. The final circuit is implemented in a 0.35 um CMOS process.

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UN NOU COMPARATOR TRIGGER SCHMITT PENTRU BIST PRIN METODA OBT

(Rezumat)

Se prezintă o nouă structură pentru un trigger-Schmitt. Noutatea constă în faptul că comparatorul prezintă o formă atipică a caracteristicii şi este astfel de folos într-o structură clasică OBT unde sunt necesare astfel de caracteristici. Articolul reprezintă o continuare a unui studiu OBT anterior. Circuitul este discutat în contextul metodei OBT modificate şi implementat într-o tehnologie CMOS standard de 0.35 µm.