BULETINUL INSTITUTULUI POLITEHNIC DIN IAŞI
Publicat de
Universitatea Tehnică „Gheorghe Asachi” din Iaşi
Tomul LVII (LXI), Fasc. 2, 2011
Secţia
ELECTROTEHNICĂ. ENERGETICĂ. ELECTRONICĂ

ON THE DESIGN OF CURRENT CONTROLLED IMPEDANCES BASED ON A VARIABLE GAIN CURRENT AMPLIFIER

BY

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Received: September 17, 2010
Accepted for publication: January 23, 2011

Abstract. A solution for a current controlled impedance based on a variable gain current amplifier is proposed. Design guidelines are discussed in detail, paying special attention to theoretical aspects and simulation results. A macromodel of the proposed circuit is presented too. The circuit solution was designed and simulated in a 0.35 um CMOS technology, using a 3.3 V power supply.

Key words: CMOS amplifiers; current scaling.

1. Introduction

In the last years analog designers paid particular attention to current-mode circuit techniques. Necessity of this techniques appears when, for severe specifications (for example when simultaneously wide bandwidth, low power consumption and low voltage operation are needed), the voltage-mode operational amplifier, which was for a long time the main building block in analog circuit design, proved to be inefficient. Furthermore voltage-mode operational amplifier circuits have limited bandwidth at high closed-loop gains

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due to the constant gain-bandwidth product. The limited slew-rate of the operational amplifier affects the large-signal, high-frequency operation. From these considerations a growing need for new, low voltage analogue techniques results (Koli *et al.*, 2003).

One way for finding another, preferably simpler, circuit realization is to use current mode circuits rather than voltage mode ones for signal processing. MOS-transistors in particular are more suitable for processing currents rather than voltages because the output signal is the current both for the common-source and common-gate amplifier configurations and common-drain amplifier configuration is almost useless at low supply voltages because of the bulk-effect present in typical CMOS-processes. Therefore, MOS-transistor circuits should be simplified by using current signals, preferably to voltage signals.

From another point of view, when signals are widely distributed as voltages, the parasitic capacitances are charged and discharged with the full voltage swing. This charging effect produces limited speed and considerable power consumption. Current-mode circuits cannot avoid nodes with high voltage swing either, but these are usually local nodes with less parasitic capacitances.

As an alternative solution to voltage-mode operational amplifier, current amplifiers provide some attractive features. They are particularly suitable for temperature sensors, photo-sensors and, in general, whenever the input source and/or the output are current signals (Palmisano *et al.*, 2000).

2. Impedance Configuration

The principle of a controlled impedance based on a variable gain current amplifier is presented in Fig. 1.

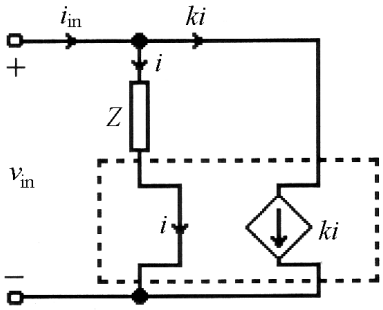


Fig. 1 – Basic principle.

By applying the Kirchhoff-I and Kirchhoff-II laws the following relations are obtained:

$$i_{in} = i + ki = (1 + k)i\,, \tag{1}$$

from which it results

$$i = \frac{i_{\text{in}}}{1+k} \tag{2}$$

and

$$v_{\text{in}} = Zi\,. \tag{3}$$

Replacing expression (2) in (3) the output impedance is obtained namely

$$Z_{\text{in}} = \frac{Z}{1+k}\,. \tag{4}$$

In relation (4) one can consider three cases for the values of the parameter *k*:

$$\begin{aligned} &\text{a) } k < -1 \Rightarrow Z_{\text{in}} < 0; \\ &\text{b) } k = -1 \Rightarrow Z_{\text{in}} \to \infty; \\ &\text{c) } k > -1 \Rightarrow Z_{\text{in}} > 0. \end{aligned} \tag{5}$$

We can conclude that it is necessary for the current amplifier to have good control linearity in a wide range around 1, ideally from –2 (when the input impedance is –*Z*) to 0 (when the input impedance is *Z*).

3. Proposed Design Solution

3.1. Scaling Technique

The scaling technique of the current (Lopey-Martin *et al.*, 2006) is based on a loop composed of four MOS transistors. The principle is illustrated in Fig. 2.

We impose that

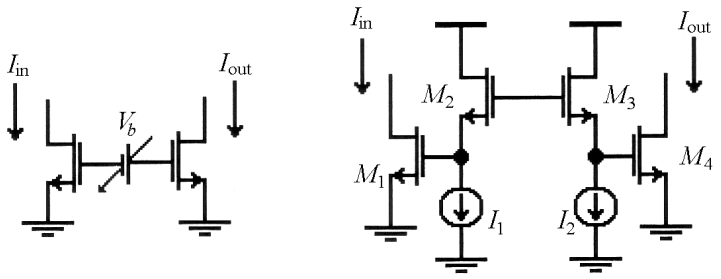
$$\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 \text{ and } \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_4. \tag{6}$$

Applying Kirchhoff-II law in Fig. 2 *b* we obtain

$$v_{gs4} - v_{gs1} = v_{gs2} - v_{gs3}. \tag{7}$$

In the following we give an intuitive analysis of the circuit. To simplify we define the control currents as follows:

$$I_1 = I - \Delta i, \;\; I_2 = I + \Delta i. \tag{8}$$



a *b*

Fig. 2 – Current scaling technique.

When $\Delta i = 0$, ($I_1 = I_2$), then $v_{gs2} = v_{gs3}$; as a consequence $v_{gs4} = v_{gs1}$ and so $I_{out} = I_{in}$. When $\Delta i < 0$ (I_1 increases and I_2 decreases), then the GS (gate to source) voltage of the M_2 transistor increases and the GS voltage of the transistor M_3 decreases. Because of the GS voltages loop, $v_{gs4} > v_{gs1}$ and $I_{out} > I_{in}$.

Following these considerations we point out three cases given in (6), also mentioning that the scaling factor can be continuously adjusted:

$$\begin{aligned} &\text{a) } \Delta i = 0 \Rightarrow I_{out} = I_{in}; \\ &\text{b) } \Delta i > 0 \Rightarrow I_{out} < I_{in}; \\ &\text{c) } \Delta i < 0 \Rightarrow I_{out} > I_{in}. \end{aligned} \tag{9}$$

3.2. Circuit Schematic

The proposed solution of the current controlled impedance based on a variable gain current amplifier is given in Fig. 3. The signal input current, i_{in} , flows through M_{n1} because of the local feedback given by M_{n1} , M_{n2} and I_1. This current is reflected through the current mirror with controllable gain formed by $M_{n1} - M_{n4}$. Since this structure reflects both the signal current and the bias one, the necessity of a replica circuit emerges, whose purpose is to extract the bias current from the total current.

The mode of operation of the amplifier with controllable gain is presented next. Through M_{n1} the total current will be $I_{bias} + i_{in}$ and this will be reflected with a k factor through M_{n4}. The cascode current mirror formed by M_{p1} , M_{p2} , M_{p1r} , M_{p2r} leads the current $k(I_{bias} + i_{in})$ in the replica circuit through the M_{p1r} , M_{p2r} branch.

In the replica circuit we have no input signal and so the bias current

which flows through the left branch is reflected with a *k* factor in the right branch.In conclusion the current of the controllable gain amplifier output is

$$i_{out} = -k\left(I_{bias} + i_{in}\right) + kI_{bias} = -ki_{in},\ (k>0). \tag{10}$$

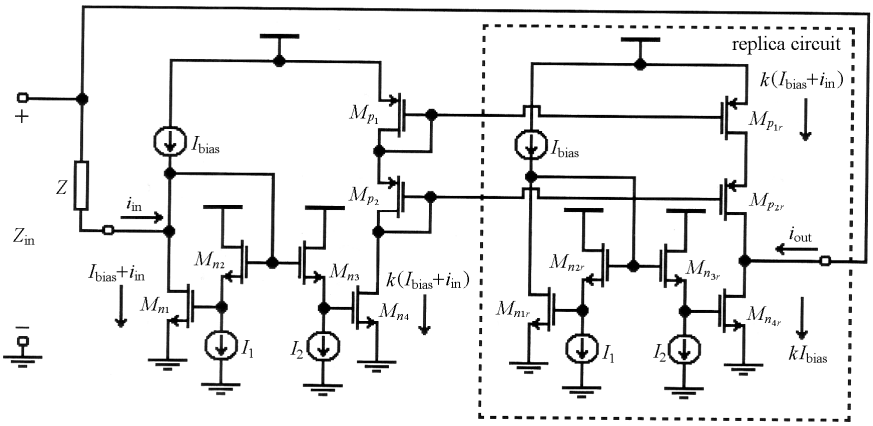


Fig. 3 – Transistor level implementation.

Thus the input circuit impedance is

$$Z_{in} = \frac{Z}{1-k},\ (k>0). \tag{11}$$

4. Simulations

The circuit was designed in a 0.35 um CMOS technology, using a 3.3 V power supply.

At equilibrium, $I_1 = I_2 = 100$ uA. We remind here the definition (8) of the control currents, where $I = 100$ uA and $\Delta i = \overline{0.60\ \text{uA}}$.

The structure simulated uses a resistive impedance of

$$Z = R = 15\ \text{k}\Omega. \tag{12}$$

The aspect ratios for all the nMOS and pMOS transistors are given in Table 1.

Table 1

	M_{n1}	M_{n2}	M_{n3}	M_{n4}	M_{p1}	M_{p2}
W, [um]	100	200	200	100	205	205
L, [um]	1	1	1	1	1	1

As a result of simulations with voltage source at the circuit input, it was observed that the circuit behaves, according to the theory for a dynamic input range of 0.3…2.6 V. A DC simulation in this interval was made for a variation of Δi factor between –60 uA and 60 uA.

The voltage/current characteristic is represented in Fig. 4, where Δi was denoted by a. Input impedance for this circuit varies from 30 k to 500 k (when Δi varies from –60 uA to 0_-) and from –30 k to –850 k (when Δi varies from –60 uA to 0_+).

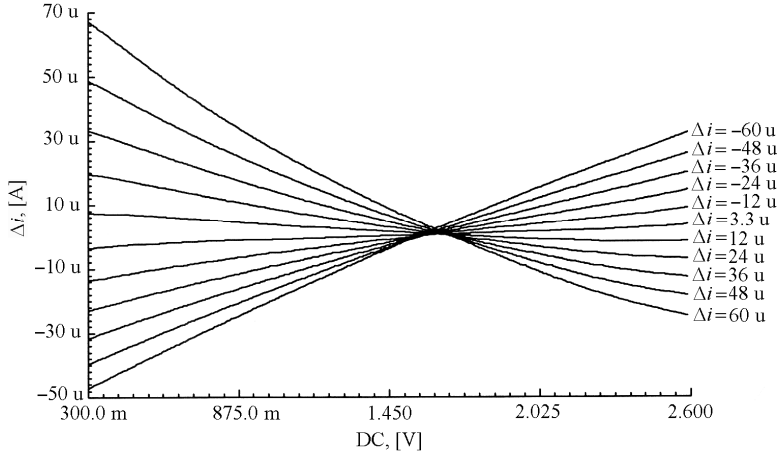


Fig. 4 – Voltage/current characteristic; DC response (Δi varies from –60 u to 60 u).

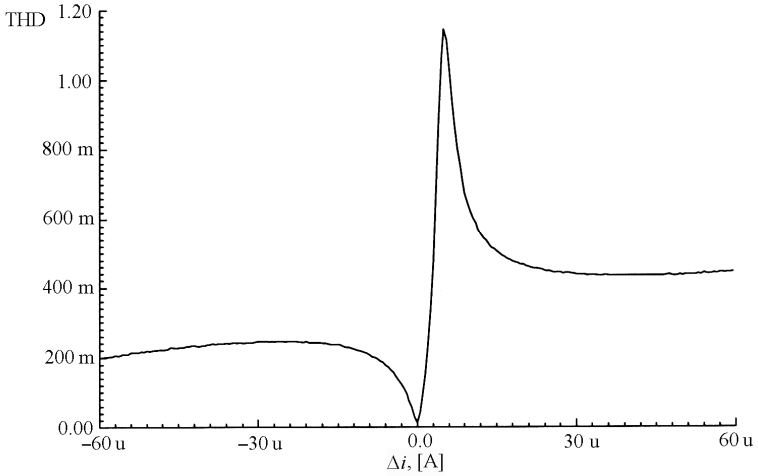


Fig. 5 – Total harmonic distortion of input current.

The total harmonic distortion of the input current (amplitude $0.1V_{pp}$ and frequency 10 kHz) for various values of Δi (from –60 uA to 60 uA) is given in

Fig. 5. It is noticeable that THD is under 1%, except the high negative impedance zone.

The impedance has been proved to be short-circuit stable. Simulations with current source at the circuit's input showed instability which means that the impedance is not open-circuit stable.

5. Macromodel of the Circuit

As it can be seen in Fig. 6, the input impedance of the variable gain current amplifier has a resistive character for a frequency within 212 MHz.

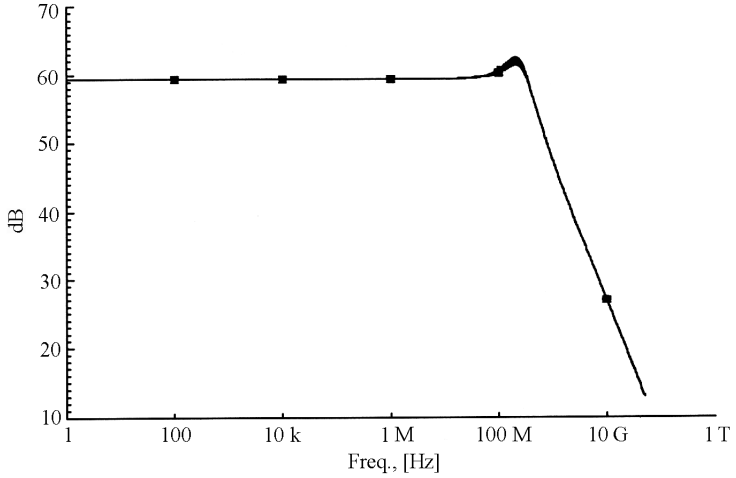


Fig. 6 – Bode plot of the input impedance of the variable gain current amplifier; ac response; Δi = 30 u, 15 u, 0, –15 u, –30 u.

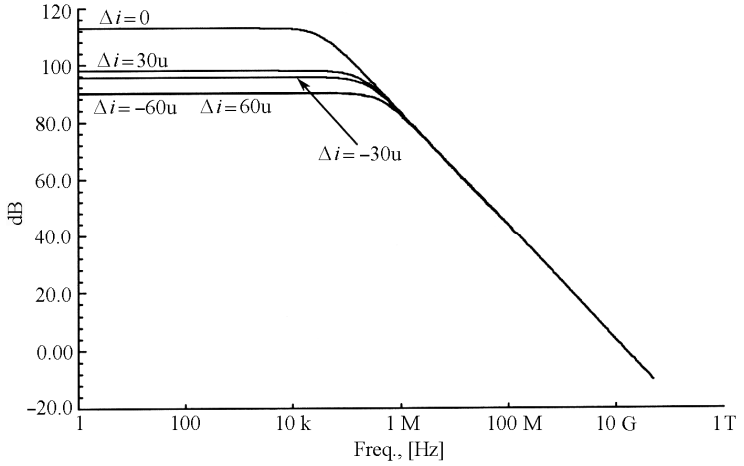


Fig. 7 – Bode plot of the input impedance of the circuit; ac response.

On the other hand, the proper circuit has a bandwith of 300 kHz (Fig.7). Therefore, the input impedance of the variable gain current amplifier may be approximated with a resistor. From the simulations it has been determined that it has the value $r \approx 1$ kΩ.

Analysing the waves from Fig. 7 one can conclude that we can add at the macromodel a capacitor from the input node to ground. The real circuit has of course a resistor from the input node to ground. The values from these components are $C \approx 1.3$ pF, $R \approx 20$ kΩ.

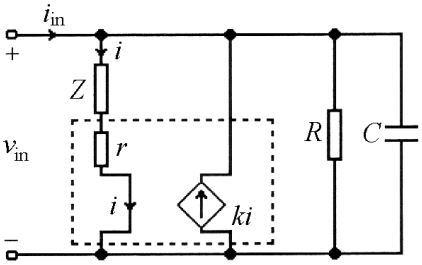


Fig. 8 – Macromodel of the circuit.

The macromodel for the implemented current controlled impedance based on variable gain current amplifier is given in Fig. 8 and the expression of input impedance is

$$Z_{in}(s) = \frac{1}{\frac{1-k}{Z(s)+r} + \frac{1}{R} + sC}. \tag{13}$$

6. Conclusions

A transistor level solution for a given realization of a current controlled impedance based on a variable gain current amplifier has been made. The control technique uses a four transistor loop operating in moderate inversion. The circuit was designed and simulated in a 0.35 um technology, with a 3.3 V power supply. Simulation results agree well with the expected results given by theory. Also a macromodel of the transistor level circuit has been realized.

The circuit uses a resistive impedance of 15 k and offers at the input a positive impedance which varies from 30 k to 500 k and a negative impedance which varies from –30 k to –850 k, providing a distorsion under 1%.

Acknowledgment. This paper was realized with the support of BRAIN "Doctoral Scholarships as an Investment in Intelligence" project, financed by the European Social Found and Romanian Government.

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REALIZAREA IMPEDANŢELOR CONTROLATE CU AJUTORUL UNUI AMPLIFICATOR DE CURENT COMANDAT ÎN CURENT

(Rezumat)

Se propune o soluţie de realizare a impedanţelor controlate prin utilizarea unui amplificator de curent cu câştig variabil. Se arată că prin această metodă se pot obţine şi scala atât rezistenţe negative, cât şi rezistenţe pozitive, în funcţie de câştigul amplificatorului de curent.

S-a proiectat un amplificator de curent cu câştig controlabil intr-o tehnologie CMOS de 0.35 um, la o alimentare de 3.3 V. Câştigul amplificatorului de curent este comandat de doi curenţi ce variază diferenţial cu $\Delta i = \overline{0,60\ \text{uA}}$ în jurul valorii de 100 uA. Astfel, prin utilizarea unei rezistenţe de 15 kΩ, s-au scalat rezistenţe între valorile –30 kΩ şi –850 kΩ şi rezistenţe pozitive în intervalul 30 kΩ...500 kΩ cu distorsiuni sub 1%.