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STUDIES REGARDING MODELING AND SIMULATION OF ELECTROSTATIC DISCHARGE PHENOMENA

BY

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Abstract. The present paper is focused on modeling and simulation aspects related to electrostatic discharge phenomena. The simulation results obtained from these investigations present the importance and influence of parasitic circuit elements on the peak and rise time of discharge current, according to electrostatic discharge (ESD) models. The program used in these studies was the Cadence software, a computational tool for design, modeling and simulation issues.

Key words: electrostatic discharge; modeling and simulation.

1. Background

The electrostatic discharge (ESD) phenomenon is defined as a transient current flow compensating the charge imbalance or the transfer of electrical charge between two bodies at different potentials, through direct contact or induced electrical field. The two main sources of electrostatic discharge events come from people and equipment. The current waveforms produced by these electrostatic perturbations can be different in shape, duration or time rising (Esmark *et al*., 2003; ESD Assoc., 2001).

ESD represents an important threat in electrical and electronical

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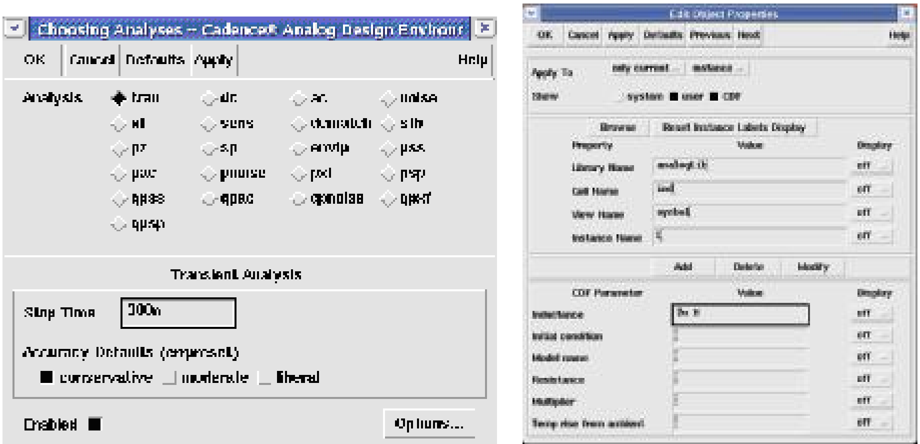
industry, because this phenomenon can be modified significantly by the electrical properties and characteristics of a semiconductor device, degrading or destroying it or may upset the normal operation of an electronic system. ESD to the device, ESD from the device or induced field discharge represent the basic ESD events which can cause important damages (Manolică & Chapalo, 2011). The electronic sector has standardized two basic models to reproduce real world electrostatic discharge events, models described by a few standards who defines the equivalent circuit structure and which are based on the electrostatic charge accumulation and storage location: Human Body Model, (HBM) and Machine Model, (MM) (ESD Assoc., 2001).

In this paper, these two ESD configurations are studied, based on modeling and simulation concepts. The electrical representation of these structures are made by *R*-*L*-*C* circuits, with variation of some important parasitic circuit elements.

2. The Software Procedure

The computational program used in the performed simulation was Cadence software 5.0, which represents an important tool for design, modeling and simulation problems of electric and electronic circuits and systems. The Cadence software, developed by Cadence Design Systems, Inc., includes some dedicated software modules, such as design module, data analysis module, physical and simulation module and can support the following analysis conditions: transient analysis (time domain condition), DC analysis, AC analysis, noise and pnoise condition and other important types of such analysis (which are briefly illustrated in Fig.1).



a *b*

Fig. 1 – Choosing simulation analysis with Cadence software.

Fig. 2 shows the general configuration for two electrostatic discharge models: Human Body Model (HBM) and Machine Model (MM). HBM is the most commonly model used for classifying the device sensitivity to ESD phenomenon and represents the discharge from the finger of a standing human person to the electronic sensitive device. This discharge arises due to the accumulation of large electrostatic charges on the body, when walks across a specified floor (ESD Assoc., 2001). The contact between the finger and the leads of an ESD system or device can have negative effects, causing device damages. Hereby, the HBM is used to simulate this ESD event. The structure is modeled through a 100 pF capacitor discharged with a switching system and a series resistor into the component with 1.5 kΩ value.

The MM illustrates a discharge alike HBM from a electrostatic charged element or object, (conductive device, tool or system) and consists of a 200 pF capacitor which is discharged into a device under test without a resistor (ESD Assoc., 2001).

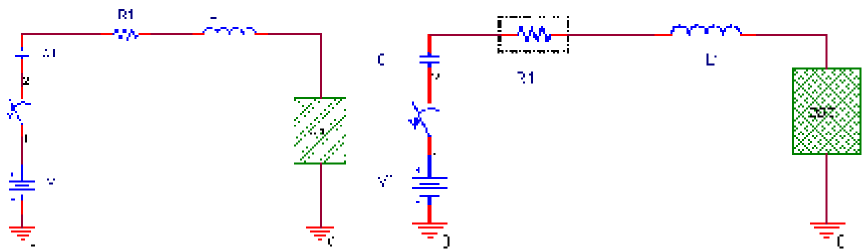
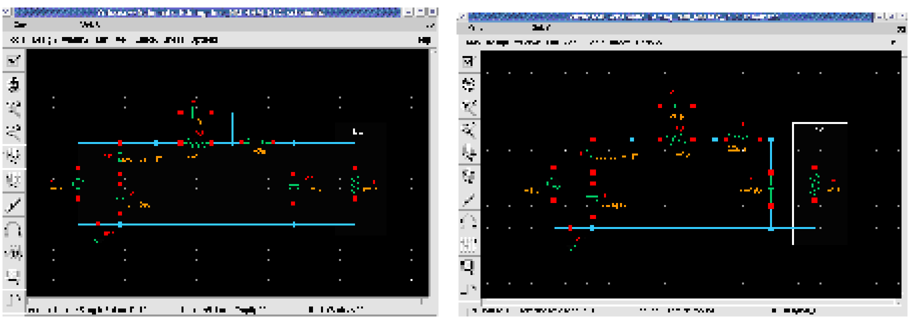


Fig. 2 – Basic ESD HBM and MM representations with *R-L-C* elements.

3. Modeling and Simulation Results

In Fig. 3 are presented the HBM and MM configurations used in these studies.



a *b*

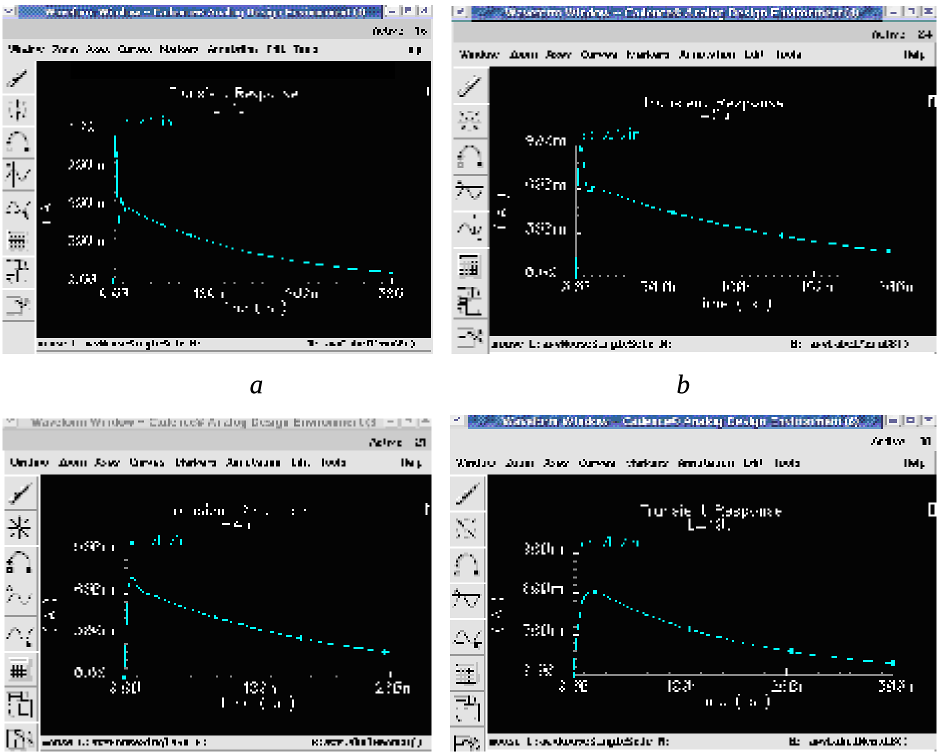
Fig. 3 – The equivalent discharge circuits used for a voltage of 1,000 V (HBM – *a*), respectively 150 V (MM – *b*).

The electric circuit for HBM contains a 100 pF capacitor, discharged by a 1.5 kΩ resistor, to generate a direct pulse similar to initial pulse generated by the human finger touching a sensitive electronic device or circuit, and a few parasitic elements (parasitic inductances and capacitors) with specific values, to describe the influence of these circuit elements for this event. The equivalent circuit for MM is similar to HBM structure, with different values of the circuit elements (200 pF capacitor and a small resistor). The values for circuit elements used in these modeling and simulation tests are illustrated in Table 1.

Table 1
The Basic Element Circuit Values

HBM	MM
C = 100 pF	C = 200 pF
R = 1,500 Ω	R = 15 Ω
L = 1 μH	L = 0.5 μH
R_{DUT} = 10 Ω	R_{DUT} = 10 Ω
V = 1,000 V	V = 150 V

In Figs. 4 and 5 are illustrated the modeling and simulation results, obtained with the Cadence software for a HBM charging voltage of 1,000 V and a MM voltage of 150 V.



a *b* *c* *d*

Fig. 4 – The HBM discharge current waveform for 1 μH (*a*), 2 μH (*b*), 4 μH (*c*) and 10 μH (*d*) parasitic inductance and 1 kV charging voltage.

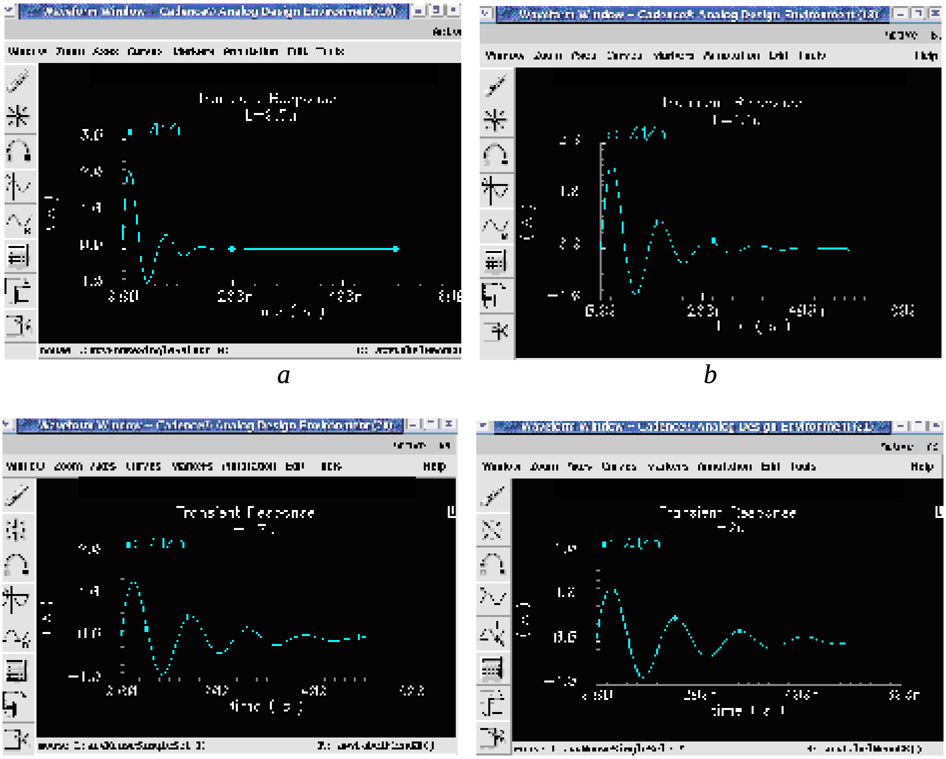


Fig. 5 – The MM discharge current for 0.5 µH (*a*), 1.1 µH (*b*), 1.7 µH (*c*) and 2 µH (*d*) parasitic inductance and 150 V charging voltage.

The current discharge associated to HBM is presented in Fig. 4, characterized by a time period of 300 ns and with 50 ns step variation (time domain simulation analysis). Fig. 4 ***a*** shows the current waveform for 1 µH parasitic inductance, *L*, and a 1,000 V voltage charging. The variation of parasitic circuit elements influences the shape and time rising of discharge current waveform for HBM event. For values of 1 µH and 2 µH of parasitic inductance, *L*, and 1,500 Ω of resistance, *R*, HBM , the current waveform is close to typical discharge current shape, specified by the dedicated ESD standards and associations. In Figs. 4 *b*, *c* and *d* are presented the simulation results for *L* = 2 µH, 4 µH and 10 µH parasitic inductance, respectively, parasitic capacitor C_1 = 1 pF and R_{DUT} = 10 Ω. The modeling and simulation discharge current associated to MM event are illustrated in Figs. 5 for a charging voltage of 150 V, R_{MM} = 25 Ω and *L* = 0.5 µH (Fig. 5 *a*), *L* = 1.1 µH (Fig. 5 *b*), *L* = 1.7 µH (Fig. 5 *c*) and *L* = 2 µH (Fig. 5 *d*) of parasitic inductance, C_{MM} = 200 pF, parasitic capacitor of 10 pF and 150 V charging voltage.

4. Conclusions

ESD arise due to the electrostatic charge accumulation. These electrostatic phenomena can create significant damages in electrical and electronic industry (mostly on semiconductor and integrated circuits and systems), bringing up to the degradation and destruction of these devices. Thus, it is necessary to avoid or diminish the accumulation of electrostatic charges to avoiding the apparition of ESD phenomena.

This work is focused on some modeling and simulation tests and researches based on electrostatic discharge events, associated to these phenomena.

The simulation results obtained with Cadence software illustrates the importance of parasitic elements from the ESD models structure, to find the most accurate and proximate discharge current waveform (rise time, shape or peak) associated to ESD events.

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STUDII PRIVIND MODELAREA ŞI SIMULAREA FENOMENELOR DE DESCĂRCARE A SARCINILOR ELECTROSTATICE

(Rezumat)

Lucrarea este conturată pe problematica modelării şi simulării fenomenelor de descărcare a sarcinilor electrostatice (ESD). Rezultatele obţinute din aceste studii se

referă la influenţa utilizării elementelor parazite de circuit din structura modelelor ESD, în vederea obţinerii caracteristicilor specifice curentului de descărcare asociat acestor fenomene. Programul utilizat în aceste încercări a fost Cadence software, un instrument computaţional de proiectare, modelare şi simulare a circuitelor şi sistemelor electrice şi electronice.