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# MIXED-SIGNAL AUTOMATIC TUNING CIRCUIT FOR INTEGRATED ANALOG FILTERS

BY

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**Abstract.** A new automatic tuning circuit for integrated analog filters which combines digital and analog control signals in the tuning loop is proposed. It is argued that in order to increase the dynamic range of an integrated filter the tuning range of the variable elements must by reduced in order to increase linearity. A reduced tuning range cannot take into account process tolerances, therefore it is extended by using switched linear elements in order to keep the overall linearity. It is stated that in order to accommodate this modification, the traditional automatic tuning circuits must include an analog to digital (A/D) and a digital to analog (D/A) converter that will be part of a digital tuning loop to perform a coarse tuning. After the coarse tuning a fine tuning is performed by an analog tuning loop which reduces the final tuning error.

**Key words:** automatic tuning circuits; integrated analog filters; mixed-signal circuits.

## 1. Introduction

In order to realize a prescribed transfer function, analog integrated filters require components with accurate values. Yet in a standard process such components are not available, and even with additional steps involving

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trimming, the devices are still subject to aging and operating conditions like temperature.

In order to circumvent the devices' tolerances, aging and change of operating conditions, the analog filter parameters must be tuned automatically by an on-chip control circuit. The tuning circuit compares some filter characteristic or parameter to a reference value or signal and generates the correction signals in order to compensate the detected errors.

Usually the reference is a fixed or periodic sinusoidal or square wave signal, but it can also be an off-chip component like a resistor which has a temperature dependence opposed to that of the on-chip capacitors.

### 1.1. Automatic Tuning Techniques

When the tuning circuit of a filter is active we can distinguish (Sun *et al*., 2002; Tsividis, 1994)

a) on-line tuning, in the case when the tuning circuit is active during normal operation of the filter;

b) off-line tuning, in the case when the tuning circuit is active in the periods of time when there is no signal at the input of the filter (*e.g*. the field fly-back time of a video signal or the time during which the terminal is out of its access frame for time-division multiple access systems).

Except for some cases, most filters have to be tuned on-line. In order to measure a filter characteristic one cannot avoid the injection of a test signal. Because the filter is operating during the automatic tuning, the designer must make sure that this test signal does not produce significant interference.

The most widely adopted technique is to use a master–slave configuration. A simplified version of the filter, that keeps the filter's most important characteristics (the ones that are to be tuned), is made part of a feedback circuit such that a parameter or characteristic is tuned by means of a control signal to a desired/reference value. The same control signal is applied to the slave, *i.e*. the main filter.

Another technique consists of using a signal chosen such that the test signal can be separated from the useful signal at the filter's output due to their orthogonality (Sun *et al*., 2002). One solution is to use the common-mode for applying the test signal in pseudo-differential filter configurations. In this case the test signal is easily separated from the useful signal, as it appears on the common-mode. The common-mode transfer function gives sufficient information to tune the filter. Another solution is to take into account the useful signal properties and to use a mostly orthogonal on it test signal. The test signal is then separated at the output of the filter.

### 1.2. Tuning Range – Dynamic Range Trade-Off

The tuning circuit must compensate the components deviations due to technology imperfections or operating conditions variability. In order to realize

that condition it must be capable of adjusting some elements of the filter in a range that can be as wide as ±50%. Typically, there is a trade-off between an element's tuning range and its linearity/dynamic range (DR).

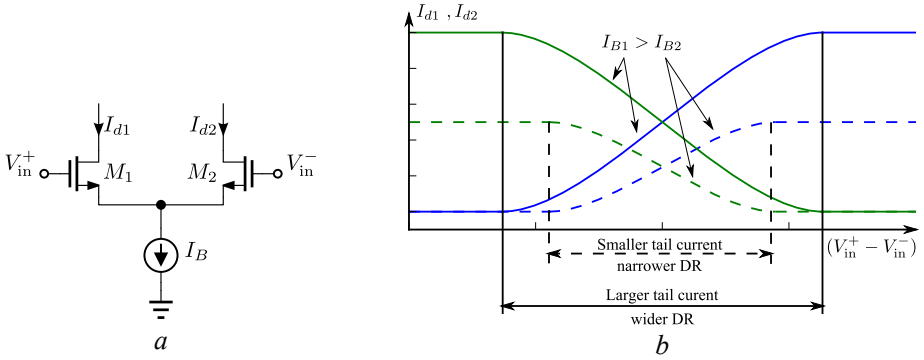



Fig. 1 – The differential stage – elementary transconductor in $G_m - C$ filters: *a* – schematic; *b* – the transistors' drain current to input voltage.

One example is the differential stage (Fig. 1 *a*). It is widely used in high-frequency $G_m - C$ filters as a transconductor. It is tuned by varying its tail current. The dependence of the transistors' currents *vs.* the input voltage is given by (Razavi, 2001)

$$I_{d1} = \frac{1}{2} I_B + \left(V_{\text{in}}^+ - V_{\text{in}}^-\right) \frac{1}{2} \sqrt{2k \frac{I_B}{2} - \left[\frac{k}{2}\left(V_{\text{in}}^+ - V_{\text{in}}^-\right)\right]^2} \quad \text{for} \left|V_{\text{in}}^+ - V_{\text{in}}^-\right| \le \sqrt{2} \sqrt{\frac{2\frac{I_B}{2}}{k}},$$

$$I_{d1} = I_B \text{ for } V_{\text{in}}^+ - V_{\text{in}}^- > \sqrt{2} \sqrt{\frac{2\frac{I_B}{2}}{k}} \text{ and } I_{d1} = 0 \text{ for } V_{\text{in}}^+ - V_{\text{in}}^- < -\sqrt{2} \sqrt{\frac{2\frac{I_B}{2}}{k}},$$

$$I_{d2} = I_B - I_{d1}.$$

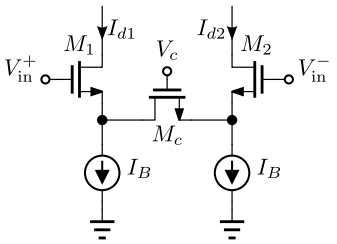



Fig. 2 – The degenerated differential stage which uses a triode-biased transistor to realize the voltage to current conversion.

We have illustrated this dependence in Fig. 1 *b* for two bias currents. It can be seen that the dynamic range (DR) depends on the tail current, therefore there is a trade-off between dynamic range and tuning range.

Another example is the source-degenerated differential pair with a triode-biased transistor for voltage to current conversion (Fig. 2). Considering that all the input voltage appears across the terminals of the degenerated transistor, we can write the following relation between the transistor's drain to source current and the transistor's balanced drain to source voltage (s. Fig. 3 *a*):

$$I_{ds} = kV_{c\text{eff}}V_{ds} \text{ for } |V_{ds}| < 2V_{c\text{eff}}$$

and

$$I_{ds} = \text{sgn}(V_{ds})\frac{k}{2}\left(V_{c\text{eff}} + \left|\frac{V_{ds}}{2}\right|\right)^2 \text{ for } |V_{ds}| \geq 2V_{c\text{eff}},$$

where

$$V_{ds} = V_{\text{in}}^{+} - V_{\text{in}}^{-},\ V_{c\text{eff}} = V_c - \frac{V_{\text{in}}^{+} - V_{\text{in}}^{-}}{2} - V_{th}.$$

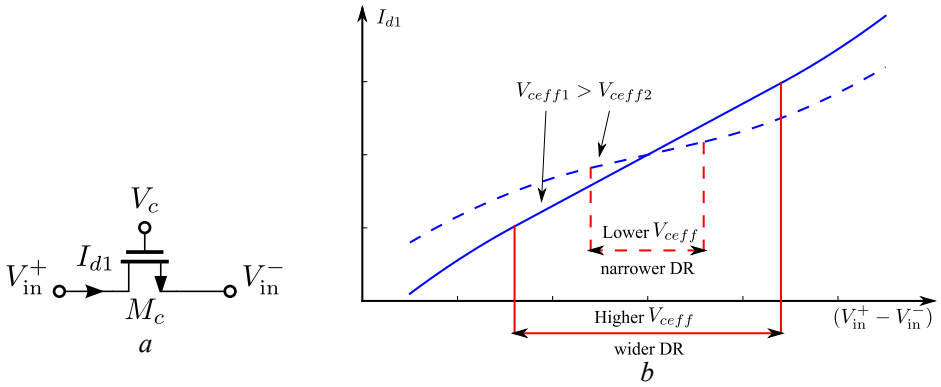



Fig. 3 – The triode-biased transistor which does the voltage to current conversion: *a* – terminal voltages and currents; *b* – the dependence of the drain *vs.* source current on the balanced drain to source voltage for the *n*MOS transistor.

Examining Fig. 3 *b* we can see the interdependence between the dynamic range and the tuning range.

Unless a linear and controllable device is available, other methods to circumvent this limitation have to be applied. One approach is to use linear devices, such as resistors or capacitors, and switches in order to obtain linear controllable devices. This way it results a discretely controllable linear device (Durham *et al.*, 1992). The limitation to this approach is ultimately the precision with which the control can be done. To obtain a precise control one has to use a large number of bits for the controlling signal (for a ±5% precision one has to use 5-bit quantization of tuning elements (Durham *et al.*, 1992)).

Another approach is to compensate the non-linearities of the active devices (Bult & Wallinga, 1987; Silva-Martinez *et al.*, 1991; Kuo & Leuciuc, 2001; Koziel & Szczepanski, 2002). All existing techniques rely on specific

device non-linearities and therefore are technology dependent. The devices can be controlled with greater precision as compared to the previous approach, but with a loss of linearity.

We propose a technique that combines the merits of the previous two approaches. It uses both programmable passive and variable active devices in order to obtain a highly linear, precisely controllable, mixed passive/active device. This combination gives the advantages of both techniques, at the expense of a more complicated tuning circuit, which contains two tuning loops – one for the generation of the discrete control signals, and the other one for the generation of the continuous control signal. Simply said, the idea of this tuning technique can be regarded as a two-stage process: first a coarse tuning is done by means of the discrete control signals, then, in the second stage, a fine tuning is done by means of the continuous control signals.

In this case the tuning loop contains an A/D converter which generates the discrete control signals. The tuned elements have in this situation the role of D/A converters with regard to the control signals.

This tuning technique (coarse plus fine) can be applied to any existing, continuous only control signal tuning loop. In this paper we will illustrate the application of this principle for a charge transfer based tuning loop, which tunes a reference transconductance to a switched capacitor simulated conductance, therefore setting a relation between the transconductance and the capacitance.

The rest of this paper is organized as follows: in Section **2** we discuss an example of a mixed passive/active device and a possible implementation of a transconductor which uses it for voltage to current conversion, in Section **3** we present the master–slave tuning circuit that overcomes the limitation of the dynamic range – tuning range trade-off by using a mixed A/D control signal; in Section **4** we show the simulation results. Section **5** draws the conclusions to this paper.

## 2. Controllable Conductance and Transconductance

The controllable conductance element used is illustrated in Fig. 4. It contains an array of switched passive resistances connected in parallel with a continuously adjustable active resistor implemented with a triode-biased transistor in series with a linearization resistor (Laximinidhi *et al*., 2009).

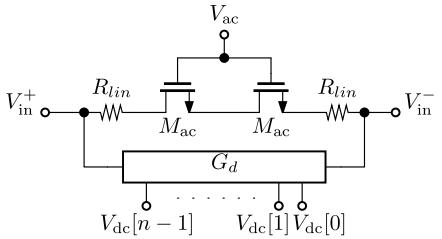



Fig. 4 – The controlled conductance which has a digital control signal together with an analog control signal.

This controllable conductance is used as degeneration in a differential stage with local feedback to improve linearity, as shown in Fig. 5. In this paper the transconductor has been described as a Verilog-A module (Listing 1).

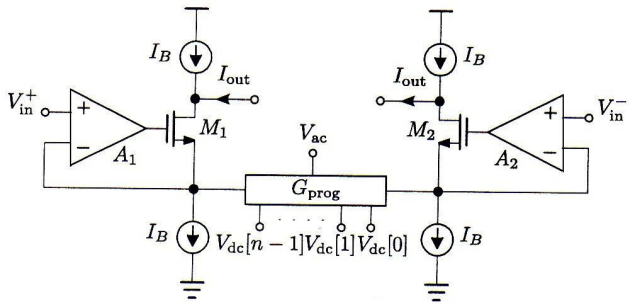



Fig. 5 – A possible implementation of the controlled transconductance.

**Listing 1**

*Verilog-A Description of the Transconductor*

```
`include "constants.vams"
`include "disciplines.vams"

`define vthresh 1.65

module linear_gm_Verilog_AMS (iout_p, iout_n, vin_p, vin_n, vc_d,
vc_a);

    output iout_p, iout_n;
    input  vin_p, vin_n, vc_d, vc_a;

    electrical iout_p, iout_n, vin_p, vin_n, vc_a;
    electrical[2:0] vc_d;

    parameter real gm_e = 10u;
    parameter real gm_a = 10u;
    parameter real rout = 10M;
    parameter real cout = 7.34f;
    parameter real vcmfb_ref = 1.65;
    parameter real gm_cmfb = 1;

    real gm_d;
    real gm;

    analog
    begin
        @(initial_step)
            gm_d = gm_e * (4*(V(vc_d[2]) > `vthresh ? 1 : 0) +
                   2*(V(vc_d[1]) > `vthresh ? 1 : 0) +
                    (V(vc_d[0]) > `vthresh ? 1 : 0));
        @(cross(V(vc_d[2]) - `vthresh, 0) or
```

```
        cross(V(vc_d[1]) - `vthresh, 0) or
        cross(V(vc_d[0]) - `vthresh, 0))
          gm_d = gm_e * (4*(V(vc_d[2]) > `vthresh ? 1 : 0) +
                 2*(V(vc_d[1]) > `vthresh ? 1 : 0) +
                 (V(vc_d[0]) > `vthresh ? 1 : 0));
      gm = gm_d + gm_a * V(vc_a);
      I(iout_p, iout_n) <+ gm * V(vin_p, vin_n) +
                           1/rout * V(iout_p, iout_n) +
                           cout * ddt(V(iout_p, iout_n));
      I(iout_p) <+ gm_cmfb *
                   ((V(iout_p) + V(iout_n)) / 2 - vcmfb_ref);
      I(iout_n) <+ gm_cmfb *
                   ((V(iout_p) + V(iout_n)) / 2 - vcmfb_ref);
  end
endmodule
```

## 3. Mixed-Signal Tuning Circuit

The automatic tuning principle relies on a master–slave topology. The automatic tuning loop adjusts the controllable transconductance to match a switched-capacitor simulated conductance.

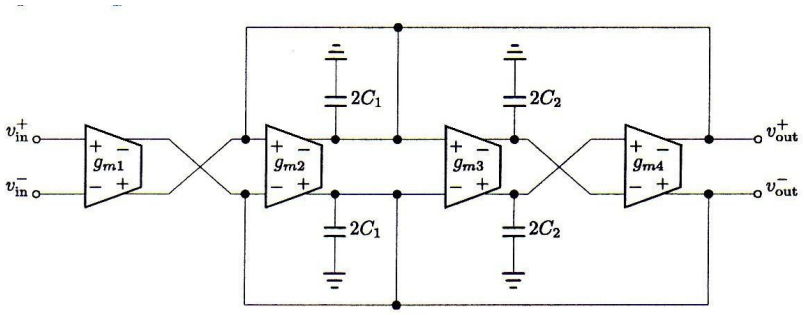



Fig. 6 – The tuned second-order bandpass filter.

The tuning process is done in two steps. At first step the digital part of the loop is active; at this step the coarse tuning is done by successive approximations such that the difference between the transconductor output current and the switched-capacitor current is minimized. After this step the digital loop is replaced by an analog loop that reduces the error signal even further by means of the analog control signal of the transconductor.

In the first phase, when the coarse tuning takes place, the digital loop which contains the A/D converter is active. In this phase the switches $K_{d1}$ and $K_{d2}$ are closed, and the switch $K_a$ is open (Fig. 7). By means of a binary search, the successive approximations register (SAR) sets the digital control signals $Q[n-1:0]$ such that the transconductance, $g_{mr}$, best approximates the value of the conductance implemented by the switched capacitor, $C_r$.

The operational amplifier, $A_1$ , is used within a low-pass active filter which extracts the mean current that results as a difference between the current injected by the $g_{mr}$ transconductor and the current injected by the simulated conductance implemented with $C_r$. The operation amplifier, $A_2$ , is in a Schmitt trigger configuration, so that its hysteresis removes the ripple due to insufficient filtering of the current injected by the capacitor $C_r$. The response of the comparator is applied into the successive approximations register. When the successive approximations converter sets the last bit, it generates the "conversion complete" (CC) command, which drives the tuning circuit into the second tuning phase.

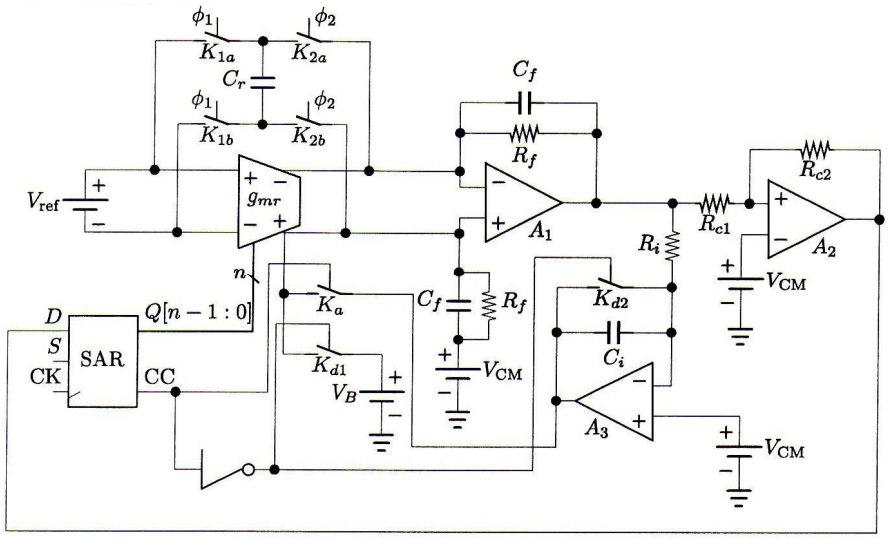
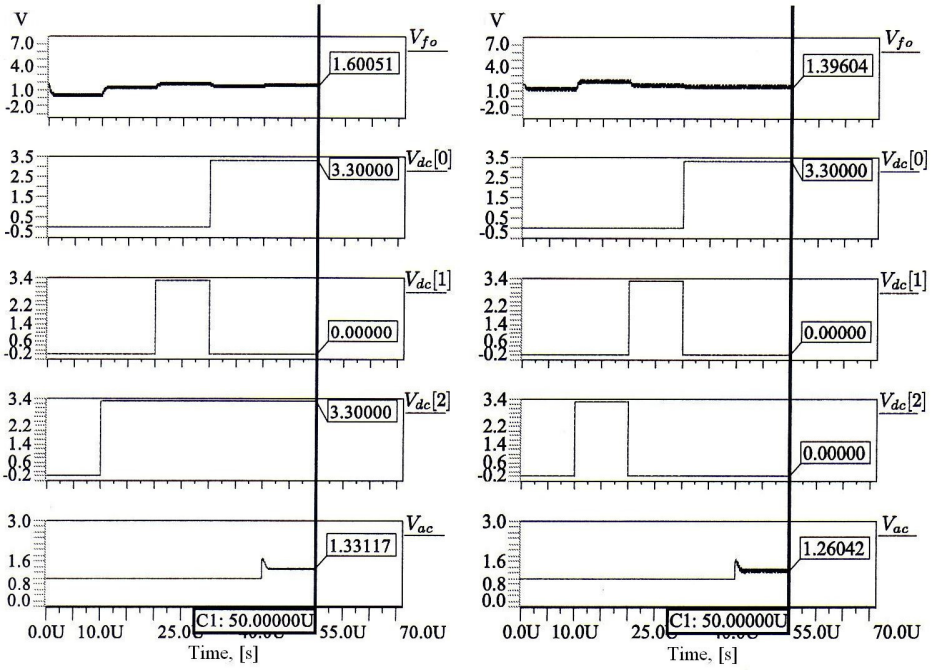



Fig. 7 – The proposed automatic tuning circuit.

In this phase the switches $K_{d1}$ and $K_{d2}$ are open, and the switch $K_a$ is closed, such that the analog tuning loop, which generates the continuous control signal, is active. This loop shares the active filter with the digital loop, to which an integrator, formed around the operational amplifier, $A_3$, is added to increase the low frequency gain of the loop in order to minimize the tuning error. The integrator also helps to filter out the high frequency components of the active filter output signal.

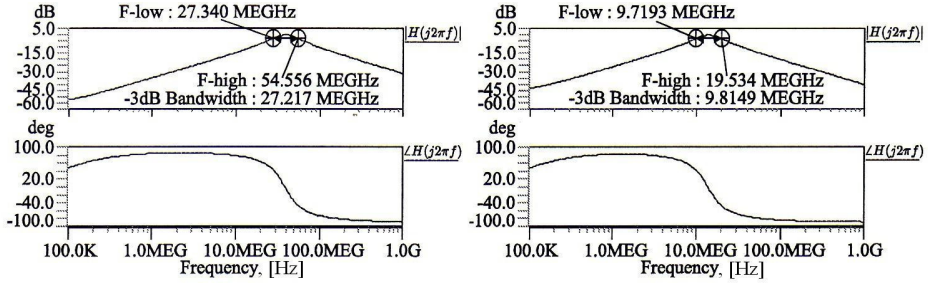
## 4. Simulation Results

Figs. 8,…,10 represent the simulation results of the proposed mixed-signal tuning circuit. The tuned filter is a second-order, bandpass filter (Fig. 6). Fig. 8 shows the transient simulation of the tuning circuit for two clock periods, $\phi_1$ and $\phi_2$.




*a* *b*

Fig. 8 – Control signals and loop active filter output for two reference signal periods, $\phi_1$ (*a*) and $\phi_2$ (*b*).




*a* *b*

Fig. 9 – Frequency characteristic of the tuned filter for two reference signal periods, $\phi_1$ (*a*) and $\phi_2$ (*b*).

In the first case the digital control signal, $V_{dc}[2:0]$, has the value "101" and the analog control signal, $V_{ac}$, has the value 1.33 V. In the second case the digital control signal, $V_{dc}[2:0]$, has the value "001" and the analog control signal, $V_{ac}$, has the value 1.28 V. The frequency response of the filter for these two cases is shown in Fig. 9. In the first case the filter has a center frequency of 40.94 MHz. In the second case it has a center frequency of 14.62 MHz. Finally, Fig. 10 shows the dependence between the filter's center frequency and the

clock period. It has a $1/x$ shape, as expected from the dependence $g_{mr}/C_r = 1$ imposed by the tuning circuit.

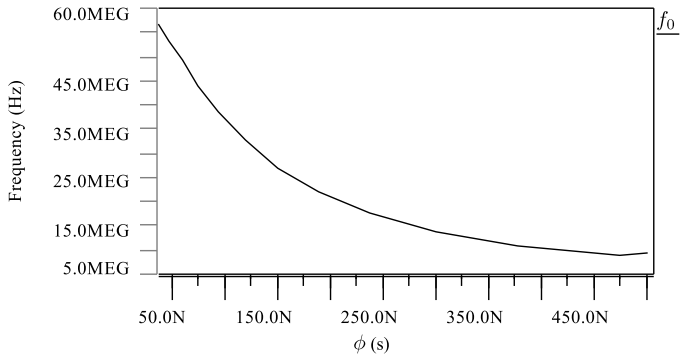



Fig. 10 – Dependence of the center frequency, $f_0$, of the tuned filter *vs*. the clock period, $\phi$.

## 5. Conclusions

In this paper we have shown that in standard technologies continuously tunable elements present a dynamic range -- tuning range tradeoff. On the other hand, the control signals of discretely tunable elements must have a large number of bits in order to fit the required precision of many applications, which is impractical when one must use many matched tunable elements. We have proposed to combine continuously tunable elements with discretely tunable elements in order to obtain a high linearity, wide tuning range, mixed control signal tunable element. We have presented the modifications that must be made to a traditional integrated analog filter tuning loop, in order to accommodate such a tunable element. The exposed ideas have been verified by simulation for a master–slave, charge-comparison based, automatic tuning loop in the case of a second-order, bandpass $G_m - C$ filter.

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## CIRCUIT DE ACORD AUTOMAT PENTRU FILTRE ANALOGICE INTEGRATE CU SEMNALE MIXTE

(Rezumat)

Se propune un nou circuit de acord automat pentru filtre analogice integrate care combină semnale digitale şi analogice în bucla de acord. Se argumentează faptul că pentru a creşte gama dinamică a filtrului integrat trebuie să se reducă gama de acord a elementelor reglabile astfel încît liniaritatea acestora să crească. O gamă de acord redusă nu poate compensa toleranţa procesului, astfel că această gamă este extinsă utilizând elemente liniare comutate pentru a menţine global liniaritatea. Se enunţă faptul că pentru a adapta circuitele tradiţionale de acord automat în vederea includerii soluţiei propuse, este necesară inserarea în buclă a unui convertor analog–digital (A/D) şi a unui convertor digital–analog (D/A) care fac parte din bucla digitală de acord pentru a realiza un reglaj brut. După ce reglajul brut a fost efectuat, se realizează un reglaj fin pentru a reduce eroarea finală de acord.