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A RAIL-TO-RAIL CMOS AMPLIFIER FOR DATA CONVERTER APPLICATIONS

BY

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Abstract. The aim of this paper is to present several circuit techniques to build up rail-to-rail CMOS amplifiers which may be successfully used in high precision A/D converters. Besides their fully differential structure these topologies also employ simple circuit techniques to increase common-mode rejection. The amplifiers have been mainly used in high signal-to-noise ratio delta-sigma modulators for audio applications based on fully differential switched capacitor techniques.

Key words: rail-to-rail amplifier; folded cascade; common-mode rejection; switched capacitor.

1. Introduction

The today's aggressive technology scaling requires for more and more innovations from analogue designers to build high performance circuitry. Particularly, the design of A/D converters proves more than ever challenging, as supply voltages are scaled down and thermal noise put severe limits on signal-to-noise ratios, while mismatches induced by small device dimensions highly affect the precision of analogue circuits.

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In these conditions, the goal of our work was to derive several circuit techniques which may be successfully used to build up high performance amplifiers. Due to their topologies, such amplifiers may be easily scaled for various technologies, representing a very important asset. Both common-mode and differential-mode behaviors of these circuits are presented, to allow for a complete image about the trade-offs required by a fully differential operation.

2. The Amplifier Architecture

The folded cascode amplifiers have been used for many years in signal processing applications, due to their relatively high DC gain and bandwidth. Moreover they do not require for complex frequency compensation techniques as a load capacitance it proves to be sufficient to ensure an adequate phase margin.

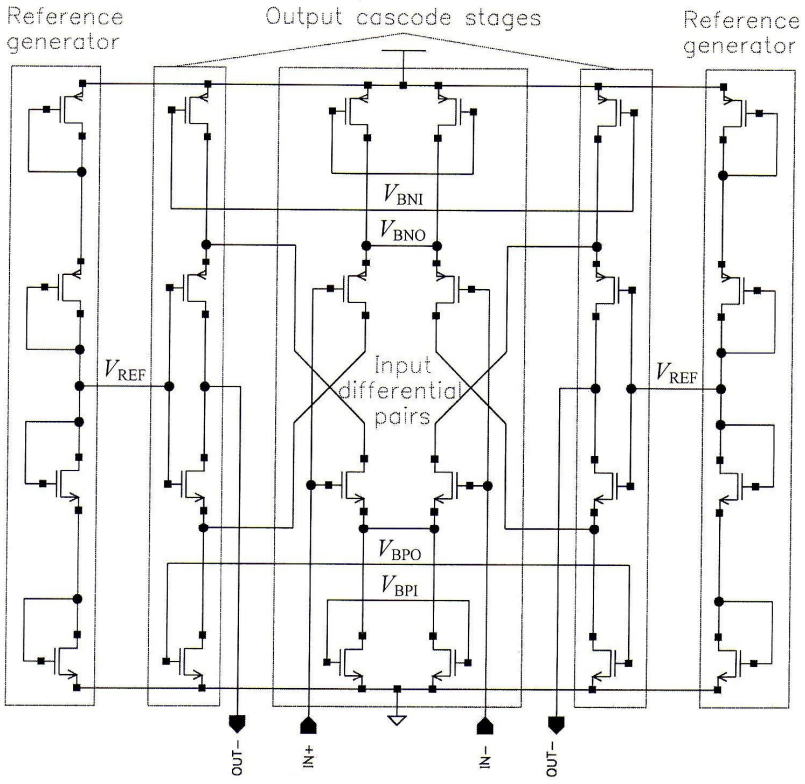

Fig. 1 – The amplifier topology.

The topology proposed by the authors is a dual input folded cascode amplifier, which may easily fulfill the gain and bandwidth constraints needed by delta-sigma modulators. The structure depicted in Fig. 1 is fully differential which also ensures high rejection of the noise on supply and ground rails.

The dual nature of inputs and outputs, employed by the usage of both *p*MOS and *n*MOS versions of input differential pairs and output cascode stages, significantly improves the output dynamic range and DC gain in differential mode.

The small signal dc amplification can be easily determined as follows:

$$A_{\mathrm{DC}} = \left(G_{M,p,\mathrm{diff}} + G_{M,n,\mathrm{diff}}\right)\left(R_{\mathrm{OUT},p} \parallel R_{\mathrm{OUT},n}\right). \tag{1}$$

In eq. (1), $G_{M,p,\mathrm{diff}}$ and $G_{M,n,\mathrm{diff}}$ are the transconductances of the input differential pairs, while $R_{\mathrm{OUT},n}$ and $R_{\mathrm{OUT},p}$ are the output resistances of the cascode stages. These resistances have high values due to the fact they are amplified version of the resistances seen in the sources of the cascode devices

$$R_{\mathrm{OUT},p} = A_{V,c,p}R_{s,p},\ R_{\mathrm{OUT},n} = A_{V,c,n}R_{s,n}. \tag{2}$$

In eq. (2), $A_{V,c,p}$ and $A_{V,c,n}$ are the intrinsic gains of the common-gate connected devices, while $R_{s,p}$ and $R_{s,n}$ are the resistances seen in the sources of these devices, in essence made up from parallel connections of drain to source resistances of the differential pairs and output stages current sources.

The reference voltage, V_{REF}, required to bias the cascode devices in the output stages, should be around half of the supply voltage. This can be achieved either using a stack of diode connected MOS transistors adequately sized, either using a resistive divider.

The bias voltages required by the current sources of the input stages, (V_{BPI} and V_{BNI}) and those required by the current sources in the output stages (V_{BPO} and V_{BNO}) may be either generated with diodes as those connected to the supply rails in the reference generators, either controlled by feedback circuits in order to improve the common-mode rejection.

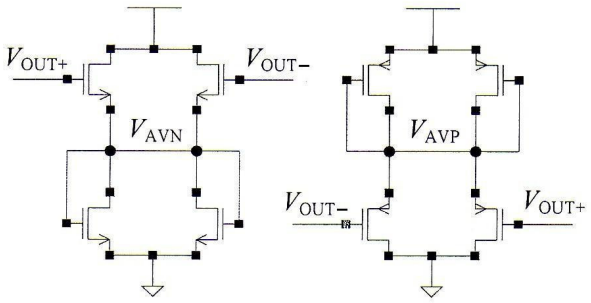

Fig. 2 – Simple voltage averaging circuits.

In addition, circuits like those depicted in Fig. 2 have been employed to increase the common-mode rejection and to ensure a rail-to-rail operation. Such circuits are based on a very simple averaging technique and provide shifted

versions of the output voltages average, V_{AVN} and V_{AVP}, which can used to control the current sources from input and/or output stages.

In a first test case, bias voltages required by the current sources in both input and output stages (V_{BPI}, V_{BNI}, V_{BPO}, V_{BNO}) have been fixed in order to get an idea about the intrinsic performances of the amplifier. In the second, respectively third configuration, the voltages V_{AVN} and V_{AVP} have been used as feedback signals to control only a pair of current sources: those in the input stages, respectively those in the output stages. In a last configuration tested, V_{AVN} and V_{AVP} have been used to control both pairs of current sources.

3. Simulation Results

The amplifier was implemented in a 0.18 um standard CMOS process and supplied by 1.8 V voltage source.

The DC simulation results for the common mode behavior of the amplifier in all four configurations are provided in Fig. 3.

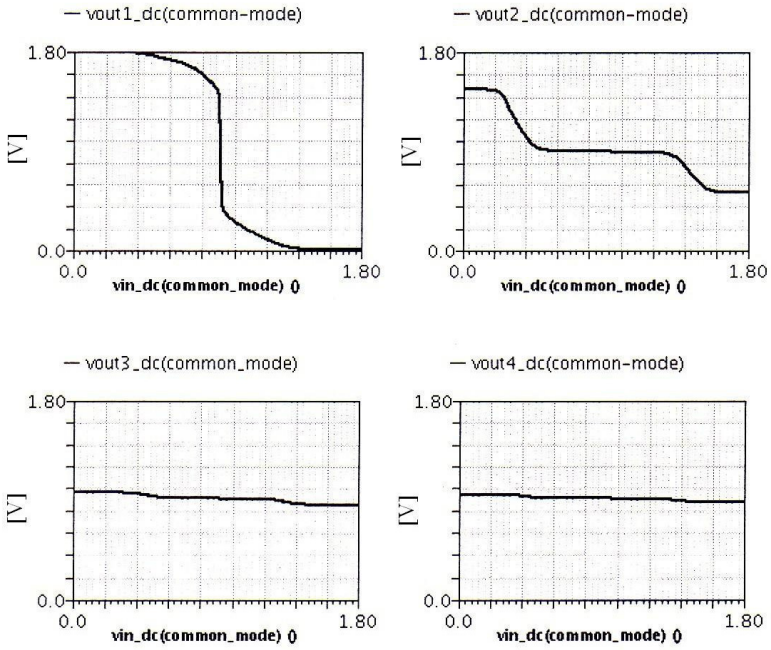

Fig. 3 – DC common-mode simulation results.

From the above results can be observed that the common mode output voltage is around 900 mV, *i.e.* half of the supply voltages, for input common-mode voltages from 0.6 V to 1.2 V, for the last three configurations, which make use of a common-mode feedback.

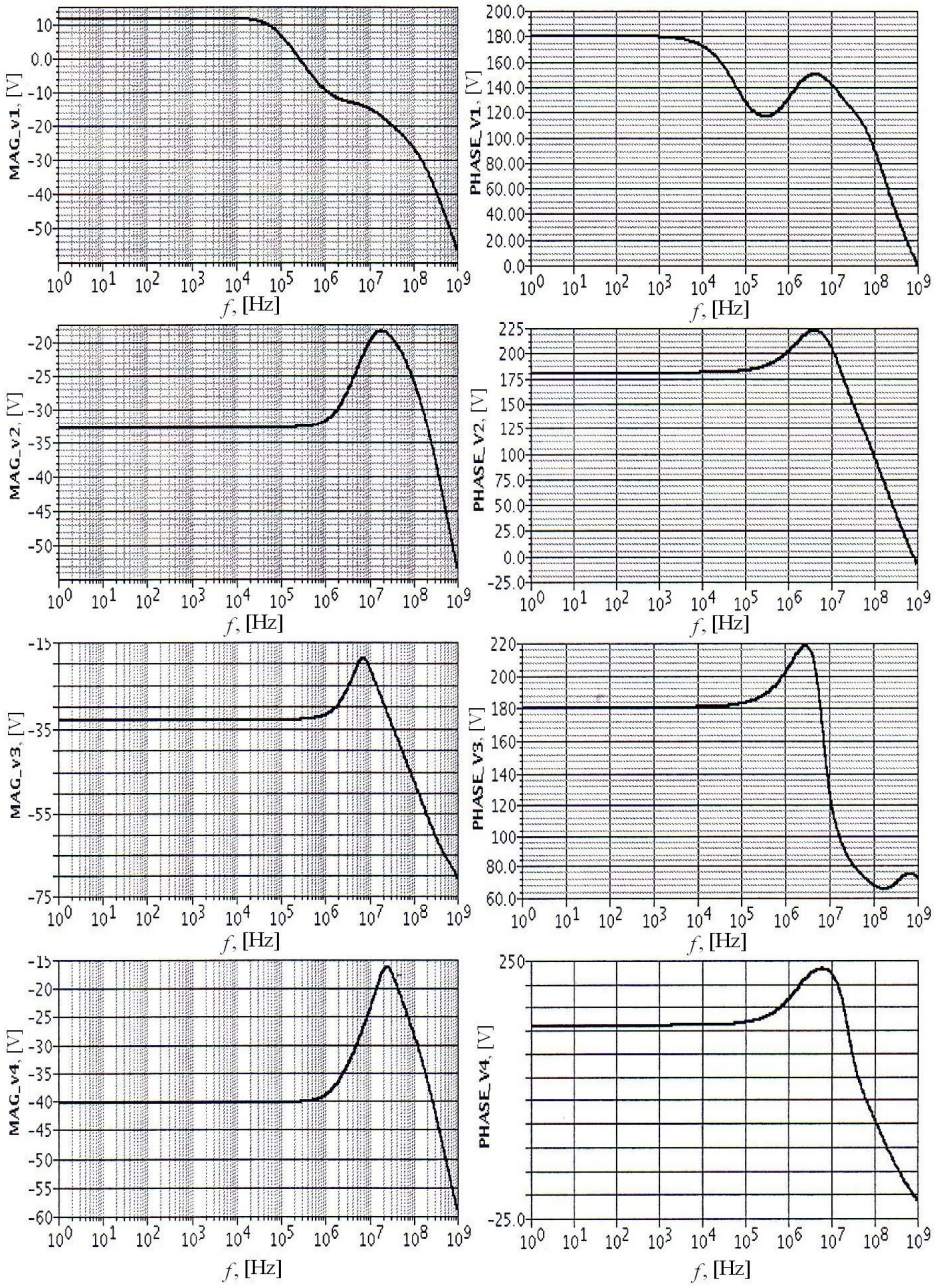

Fig. 4 – AC common-mode simulation results.

The results of the AC simulation for the common-mode, respectively differential–mode behavior, are presented in Fig. 4, respectively Fig. 5, for all configurations discussed.

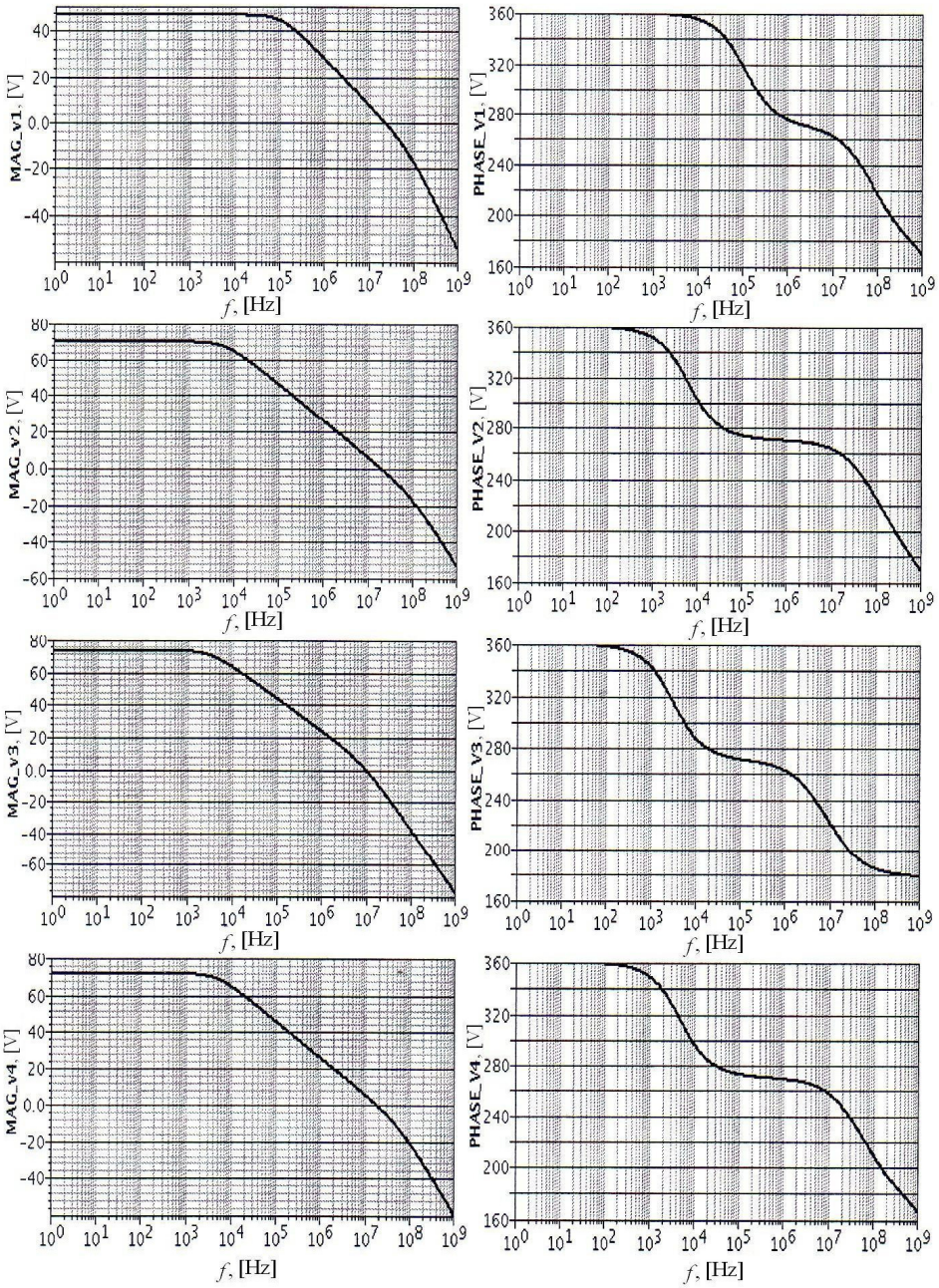

Fig. 5 – AC differential-mode simulation results.

The AC simulations were performed for a 10 pF load capacitance on each output. A summary of the performances obtained are presented in Table 1.

Table 1
Different Configurations Performances

	Differential Mode Gain-Bandwidth, [MHz]	Differential Mode Phase Margin	Common Mode Gain	Common Mode Gain Margin
V1	40.4	61.2	+11.4	56.6
V2	36.5	68.5	–32.9	50.8
V3	14.7	33.6	–33.1	81.5
V4	31.7	58.3	–40.3	55.7

Based on the comparison of the above results, the fourth configuration seemed to provide the best trade-off between common-mode and differential-mode performances. This type of amplifier has been used in a switch capacitor implementation of a high signal-to-noise ratio delta-sigma modulator.

Unfortunately, the very simple common-mode feedback circuits depicted in Fig. 2 have the drawback of relatively high variation levels of the output common-mode voltages with process and temperature, in our case 100 mV around the desired value of 900 mV. For situations where a maximum output dynamic range is required in the presence of process and temperature variations, circuit techniques like those in Fig. 6, may be used. These circuits

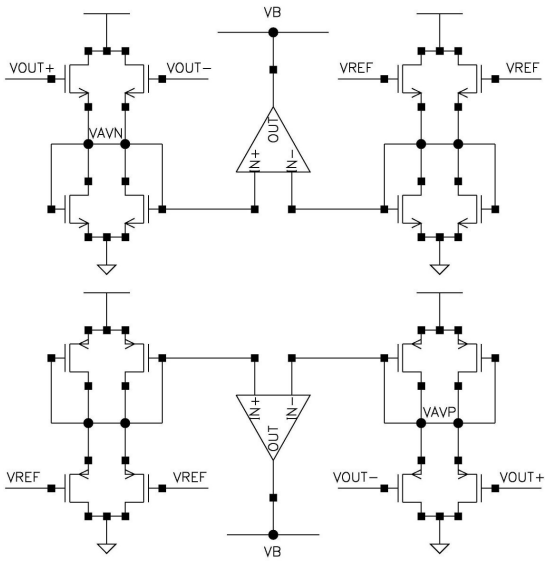

Fig. 6 – Improved common-mode feedback circuits.

perform a comparison between the shifted average value of the output voltages and a shifted version of the reference voltage as well, providing feedback voltages (V_B) which may be used to fully or partially control the current sources from the main amplifier. Yet, it should be pointed out that such circuits have to be carefully designed, as the common-mode feedback loop may become easily unstable due to the increased number of stages in the feedback path.

4. Conclusions

Several circuit techniques have been proposed to build up high performance rail-to-rail amplifiers for standard CMOS processes, together with simulation results which prove their validity and usefulness.

Due to the topologies they have, such amplifiers may be easily scalable on various technologies. The proposed amplifiers have been successfully used to build switched capacitor integrators for discrete delta-sigma modulators.

Further research will focus on the design of improved common-mode feedback circuits and on the possibilities to reduce the supply voltage.

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AMPLIFICATOR RAIL-TO-RAIL DE TIP CMOS PENTRU CONVERTOARE DE DATE

(Rezumat)

Sunt prezentate câteva tehnici de construcţie a unor amplificatoare rail-to-rail de tip CMOS. Structurile circuitelor sunt prezentate împreună cu rezultatele simulărilor ce atestă validitatea şi utilitatea lor.

Topologia de bază reprezintă în esenţă un amplificator complet diferenţial de tip cascodă împăturită cu structură dual ă (*p*MOS şi *n*MOS). Sunt prezentate şi discutate câteva tehnici pentru asigurarea unei bune rejecţii de mod comun şi desensibilizarea nivelului de mod comun la ieşire, la variaţia procesului şi a temperaturii. Astfel de amplificatoare au fost utilizate de către autori în construcţia unor integratoare cu capacităţi comutate din componenţa unor modulatoare delta-sigma discrete.