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ON THE *RLC* MODEL OF A CMOS TRANSISTOR ONLY SIMULATED INDUCTOR

BY

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Abstract. A differential topology of CMOS transistor only simulated inductor with variable self resonant frequency is studied. Taking into account the charge based capacitance model for MOSFET transistors, a more accurate *RLC* equivalent model is proposed for this topology. Besides, this model is validated by means of simulations for two particular implementations in the frequency range 0.5…6 GHz. Minimum and maximum errors of 3.51% and, respectively, 14.05% are obtained for the lowest and highest testing frequencies, the model being more accurate for lower frequencies. The simulations were carried out in 0.18 um UMC CMOS process.

Key words: active inductor; CMOS; gyrator; RF; transcapacitance.

1. Introduction

The transistor only simulated inductors (TOSI) have been extensively studied during the last two decades, many architectures being proposed in literature. Envisaging RF applications, most of them are gyrator based topologies, usually implemented with two (Ismail *et al*., 1999; Wu *et al*., 2000;

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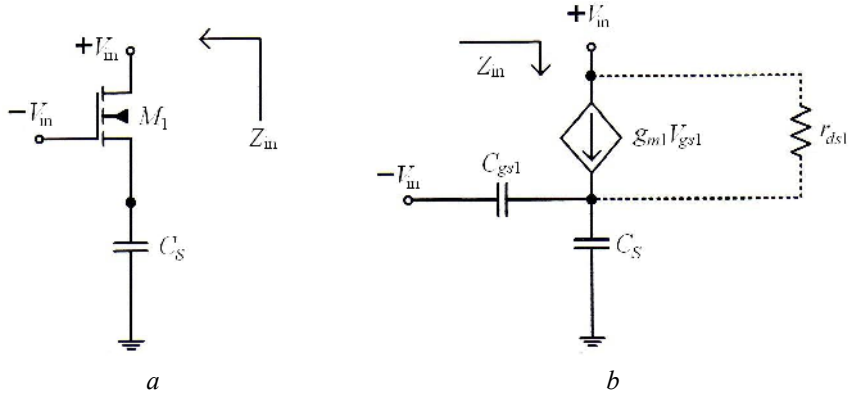
Thanachayanont, 2000) or three (Karşilayan & Schaumann, 2000; Ngow & Thanachayanont, 2003) transistors. In this case, the transistor parasitic capacitor, C_{GS} , is used as gyrator loading capacitor. The simulated inductors implemented with only one transistor (Sackinger & Fischer, 2000; Ler *et al*., 2008) are rather based on an inductive effect obtained at the circuit input than the gyrator theory.

Implemented in different technologies (GaAs, SiGe, CMOS), the main advantages of TOSI structures are the small number of transistors and low chip area, thanks to the lack of on-chip capacitors. Having small parasitics, such circuits can reach high self resonant frequencies, in the GHz domain, with relatively small power consumption. The most significant drawback is a supplementary noise contribution, the price for noise minimization being an increase in power consumption. Even in this case, such topologies are attractive for RF design, a wide range of applications being covered: active bandpass filters (Liang *et al*., 2005), VCO (Wei *et al*., 2008), CCO (Wu *et al*., 2001), power dividers (Lu *et al*., 2005) and low noise amplifiers (Hampel *et al*., 2009).

2. Single-Ended Active Inductor

The capacitive source degenerated active inductor used in our research is presented together with the small signal equivalent circuit in Fig. 1. Its (simplified) input admittance is expressed by

$$Y_{\text{in}}(s) \approx -g_{m1} + \frac{1}{\frac{1}{g_{m1}} + s\frac{C_S}{g_{m1}^2}}. \tag{1}$$



a *b*

Fig. 1 – Single-ended active inductor (Ler *et al*., 2008).

As it can be noticed, the active inductor has an equivalent circuit consisting of one real inductor in parallel with a negative resistance. This is the reason why such topology can be used to emulate the inductive behavior, as

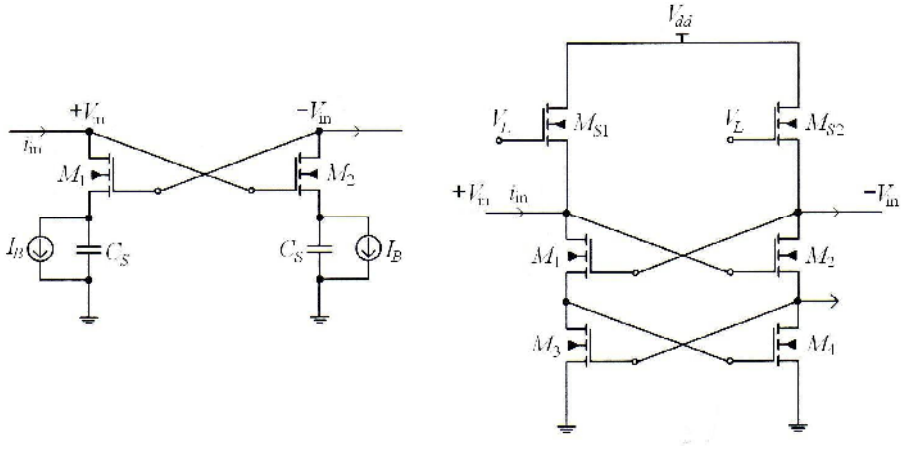
proposed by Ler *et al*. (2008). However, this circuit is not a gyrator (Andriesei *et al*.) since the output impedance is not seen inverted at the input.

Due to the intrinsic negative resistance, a supplementary positive resistance must be added to the input node in order to insure unconditional circuit stability for any supply source.

3. *RLC* Model for Differential Active Inductor

The equivalent differential topology corresponding to the previous single ended circuit is shown in Fig. 2 *a*. Such a structure was already reported as a negative capacitance (Galal & Razavi, 2003) when using floating source capacitors. In the meantime, a second version of differential topology, consisting of two cross-coupled pairs, was proposed (Ler *et al*., 2008) and is shown in Fig. 2 *b*. The circuits are different since the second one has four voltage controlled current sources while being attacked in current. The input impedance corresponding to the second circuit is

$$Y_{\text{in}}(s) \approx \frac{1}{2}\left(g_{m_{S1}} - g_{m1} + \frac{1}{\dfrac{g_{m1}-g_{m3}}{g_{m1}^2} + \dfrac{sC_{S1}}{g_{m1}^2}} \right). \tag{2}$$



a *b*

Fig. 2 – Differential active inductors.

The inductor in Fig. 2 *b* has good frequency capability, with the main advantage of easier DC biasing. However, since the architecture contains cross-coupled transistors pairs, it suffers from the impossibility of tuning the self resonant frequency tuning, the voltage V_L setting the inductor quality factor only. In this regards, a supplementary accumulation-mode MOS varactor (C_S)

was added to the source of $M_{1,2}$, its capacitance value being controlled by V_{ctrl} (Fig. 3). $M_{1,2}$ gates were decoupled for reasons of independent biasing, R_G being implemented with off transistors. Therefore, the frequency tuning capability is greatly improved, the circuit having the possibility of tuning both self resonant frequency (V_G, V_{ctrl}) and quality factor (V_L). In addition, $M_{\text{S1,2}}$ were implemented with PMOS transistors to obtain smaller node parasitic capacitances while taking advantage of smaller biasing voltages. However, the size of $M_{\text{S1,2}}$ must be carefully chosen in order to insure circuit stability. Both supplementary control voltages, V_G and V_{ctrl}, are introduced in order to validate the *RLC* model only.

Considering the charge based model for MOSFET transistor capacitance network and taking into account the transistor transcapacitances, a more accurate expression for the inductor input impedance is proposed namely

$$Z_{\text{in}}(s)=\frac{as+b}{s^2+cs+d}, \tag{3}$$

$$\begin{cases} a=2\dfrac{C_{s1}+C_{d3}+C_{gg3}+2C_S}{\left(C_{gg1}+C_{d1}+C_{dMS}\right)\left(C_{s1}+C_{d3}+C_{gg3}+2C_S\right)-\left(C_{gs1}+C_{sg1}-C_{ds1}-C_{sd1}\right)^2}, \\ b=2\dfrac{g_{m1}-g_{m3}+g_{ds1}+g_{ds3}+g_{mb1}}{\left(C_{gg1}+C_{d1}+C_{dMS}\right)\left(C_{s1}+C_{d3}+C_{gg3}+2C_S\right)-\left(C_{gs1}+C_{sg1}-C_{ds1}-C_{sd1}\right)^2}, \\ c=\dfrac{\left(C_{gg1}+C_{d1}+C_{dMS}\right)\left(g_{m1}+g_{ds1}+g_{ds3}+g_{mb1}-g_{m3}\right)}{\left(C_{gg1}+C_{d1}+C_{dMS}\right)\left(C_{s1}+C_{d3}+C_{gg3}+2C_S\right)-\left(C_{gs1}+C_{sg1}-C_{ds1}-C_{sd1}\right)^2}+ \\ +\dfrac{\left(C_{s1}+C_{d3}+C_{g3}+2C_S\right)\left(G_{MS}+g_{ds1}-g_{m1}\right)}{\left(C_{gg1}+C_{d1}+C_{dMS}\right)\left(C_{s1}+C_{d3}+C_{gg3}+2C_S\right)-\left(C_{gs1}+C_{sg1}-C_{ds1}-C_{sd1}\right)^2}+ \\ +\dfrac{\left(C_{gs1}+C_{sg1}-C_{ds1}-C_{sd1}\right)\left(g_{mb1}+2g_{ds1}\right)}{\left(C_{gg1}+C_{d1}+C_{dMS}\right)\left(C_{s1}+C_{d3}+C_{gg3}+2C_S\right)-\left(C_{gs1}+C_{sg1}-C_{ds1}-C_{sd1}\right)^2}, \\ d=\dfrac{g_{mb1}G_{MS}+g_{m1}g_{m3}+g_{ds1}g_{ds3}+G_{MS}\left(g_{m1}-g_{m3}\right)+g_{ds1}\left(G_{MS}-g_{m3}\right)+g_{ds3}\left(G_{MS}-g_{m1}\right)}{\left(C_{gg1}+C_{d1}+C_{dMS}\right)\left(C_{s1}+C_{d3}+C_{gg3}+2C_S\right)-\left(C_{gs1}+C_{sg1}-C_{ds1}-C_{sd1}\right)^2}, \end{cases} \tag{4}$$

$$C_s=C_{js}+C_{ss},\quad C_d=C_{jd}+C_{dd}. \tag{5}$$

In relations (3),…,(5), C_s, C_d and C_{gg} represent the total capacitances seen into the transistor source, drain and gate terminals, C_{ds}, C_{sd}, C_{gs}, C_{sg} are the transistor transcapacitances and C_S represents the varactor capacitance value.

Taking into account that the input impedance of an *RLC* parallel resonator has the form

$$Z_{\text{in}}(s) = \frac{s\dfrac{1}{C} + \dfrac{r_S}{LC}}{s^2 + s\dfrac{L + Cr_P r_S}{LCr_P} + \dfrac{r_S + r_P}{LCr_P}}, \tag{6}$$

the *RLC* equivalent model for this active inductor topology is obtained as shown in Fig. 4.

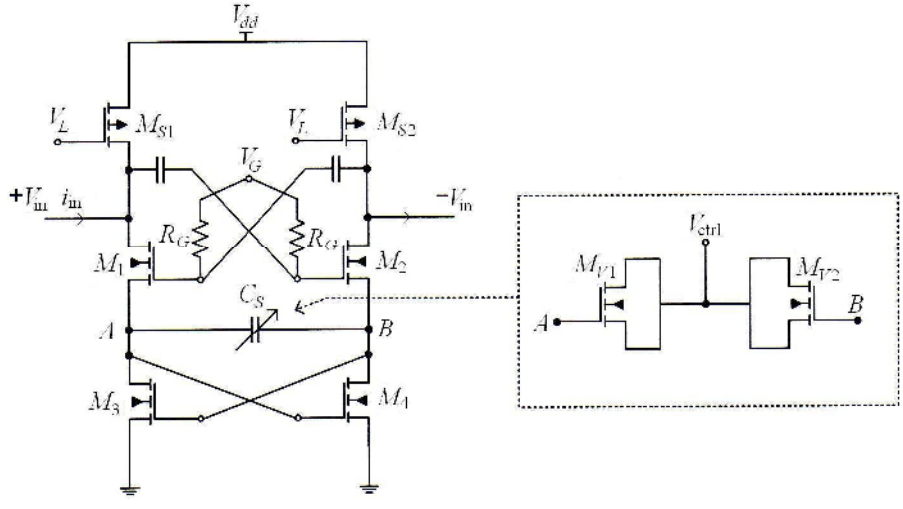


Fig. 3 – Differential active inductor with improved tuning capability and equivalent *RLC* passive model.

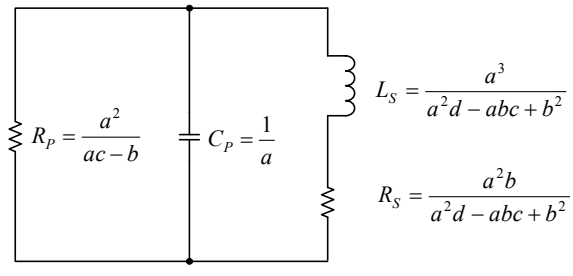


Fig. 4 – Equivalent *RLC* passive model proposed for TOSI.

4. *RLC* Model Validation for Differential Active Inductor

In order to study the accuracy of the *RLC* model proposed in Fig. 4, the active inductor topology shown in Fig. 3 was designed in two versions, with small (3 μm/0.25 μm) and large transistors (10 μm/0.25 μm), respectively. Both circuits were tuned at seven frequencies between 0.5 GHz and 5 GHz and the biasing points were extracted in Cadence. Then, the transistors parameters were used to compute the *RLC* resonator elements according to the values given in

Fig. 4, the results being summarized in Table 1. Finally, the frequency responses corresponding to *RLC* model and active inductor are compared in Figs. 5 and 6.

Table 1
TOSI Active Inductor and RLC Equivalent Model

	V_L V	V_G V	C_S fF	$f_{0,\text{TOSI}}$ GHz	L_S nH	r_S Ω	r_P kΩ	C_P fF	$f_{0,\text{RLC}}$ GHz	Error %
Circuit 1	0.97	1.2	250	0.57	4,881	1,065	80.03	15	0.59	3.51
	0.54	1.6	250	1.15	1,194	532	104.76	15.1	1.19	3.48
	0.53	1.6	150	1.46	728	530	43.93	15.1	1.52	4.11
	0.56	1.6	80	1.96	412	537	95.91	14.7	2.05	4.59
	0.58	1.6	40	2.65	228	541	67.9	14.3	2.80	5.66
	0.61	1.6	20	3.46	136	548	49.18	13.6	3.72	7.51
	0.64	1.6	10	4.31	89	556	30.34	12.7	4.77	10.67
Circuit 2	0.98	1.2	250	0.99	480	325	25.19	48	1.05	6.06
	0.82	1.33	250	1.44	224	228	29.59	49.1	1.52	5.55
	0.56	1.6	250	2.02	116	162	49.64	48	2.14	5.94
	0.57	1.6	150	2.52	75	163	23.29	47.2	2.68	6.35
	0.60	1.6	80	3.24	46	165	21.18	45.1	3.50	8.02
	0.63	1.6	40	4.10	29	167	11.56	42.3	4.57	11.46
	0.66	1.6	20	4.91	21	170	7.76	39	5.60	14.05

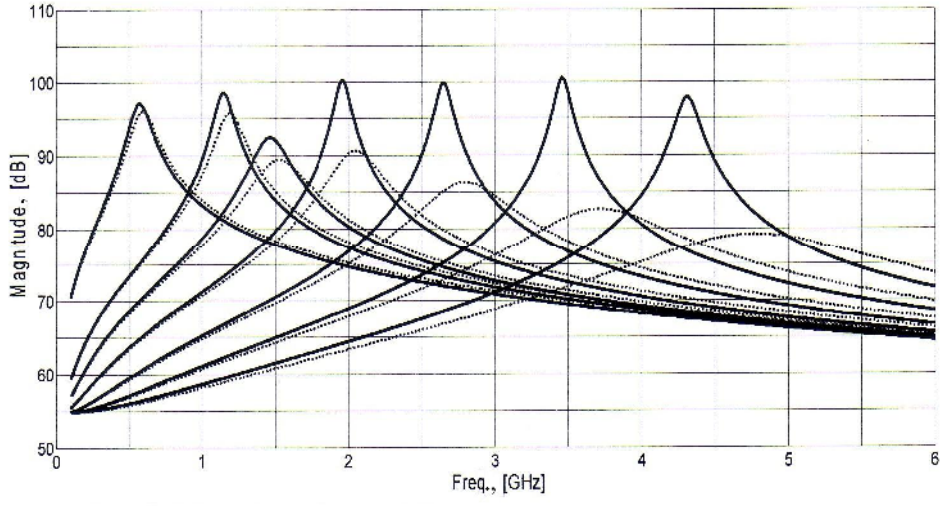


Fig. 4 – TOSI and *RLC* model frequency response for the first circuit.

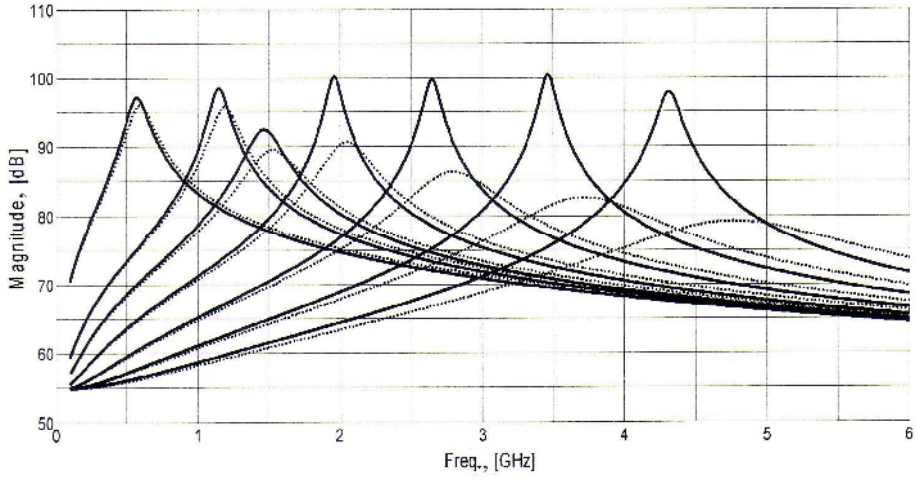


Fig. 5 – TOSI and *RLC* model frequency response for the second circuit.

Although not figured, it is interesting to notice that the current consumption is approximately constant when the quality factor is tuned. This is not the case of active inductors implemented with extra negative resistances where any improvement of the quality factor can be obtained with extra current consumption only. In this last case, the current consumption always increases as the quality factor is improved.

5. Conclusion

A passive equivalent *RLC* model was proposed and validated by means of simulations for one particular topology of CMOS source degenerated active inductor. The simulation results prove that the *RLC* model accuracy increases by using the MOS transistor model based on transcapacitances and decreases with frequency.

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STUDIU CU PRIVIRE LA MODELUL *RLC* AL UNEI INDUCTANȚE ACTIVE CMOS DE TIP TOSI

(Rezumat)

Se studiază o topologie diferențială de inductanță simulată, implementată în tehnologie CMOS numai cu tranzistoare şi cu frecvența proprie de rezonanță variabilă. Ținând cont de modelul tranzistorului MOSFET bazat pe rețeaua nereciprocă de capacități parazite, este propus un model *RLC* echivalent mai precis. În plus, acest model este validat prin simulări în domeniul de frecvență 0.5...6 GHz pentru două configurații particulare. Erori extreme, de 3.51% şi 14.05%, sunt obținute pentru frecvența cea mai joasă, respectiv cea mai înaltă de test, modelul dovedindu-se mai precis la frecvențele joase. Simulările au fost realizate în tehnologia CMOS UMC 0.18 um.