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ULTRA LOW VOLTAGE THREE STAGE SCALABLE FULLY DIFFERENTIAL AMPLIFIER

BY

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Abstract. A new approach for designing an ultra low voltage (ULV) three-stage fully-differential amplifier, using the CMOS inverter as a basic design element is proposed. Taking the advantage of the full control possibilities of both types of transistors offered by a triple well technology, such amplifiers may be designed to operate at very low supply voltages and with small power consumption. A rail-to-rail amplifier is presented and design constraints are discussed, when dealing with a 0.6 V supply voltage. The circuit was designed for a triple-well 0.18 μm CMOS process with V_{thn} and $V_{thp} \approx 0.41$ V and may be used in applications which require very high DC gains.

Key words: ultra low voltage; inverter-based; scalable amplifier; common mode compensation.

1. Introduction

In the modern days, the continuous scaling of the minimum channel length of MOS transistors requires the reduction of supply voltage well below 1 V, in order to maintain the reliability of the devices. On the other hand, the threshold voltages have to remain at rather high values in order to reduce the

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leakage. These constraints result in a design conflict that can be overcomed, as presented in this work, with a proper control of the bulk to source voltage.

The idea of using both the gate and the body as signal and/or control inputs, in a low voltage environment, was illustrated before by Chatterjee *et al*. (2005), Ferreira *et al*. (2007) and Zabihian *et al*. (2007), but this paper presents a scalable type of circuit, that can be easily modified to suit various design specifications with no impact over the DC operating points and with predictable performances. The amplifier employs three inverting gain stages and Reversed Nested Miller frequency compensation as reported by Garimella *et al*. (2010).

A review of the CMOS inverter and all inverter-based sub-circuits used in the amplifier are given in Section **2**. The circuit topology along with the key design parameters are presented in Section **3**. The simulation results of the proposed circuit are given in Section **4** and, finally, the conclusions of this work are stated in Section **5**.

2. ULV Inverter-Based Scalable Structures

The idea of a scalable inverter-based structure is that any CMOS inverter may be regarded as a transconductor, which makes it feasible for deriving gain stages and other useful circuits needed by an amplifier. Once we know the electrical characteristics of a sample CMOS inverter, we may easily derive the electrical characteristics of a parallel connection of any number of inverters identical with that sample. Next, we will denote as a *k*-scaled inverter a parallel connection of *k* inverters, identical with the sample used as a reference.

In Fig. 1 is depicted a sample CMOS inverter and its simplified small signal equivalent model. The transconductance, output resistance and input gate capacitance, derived from the small signal model of n-type and p-type transistors, are equal to $G_m = G_{mn}+G_{mp}$, $R_0 = R_{0n} \parallel R_{0p}$, $C_G = C_{Gn}+C_{Gp}$.

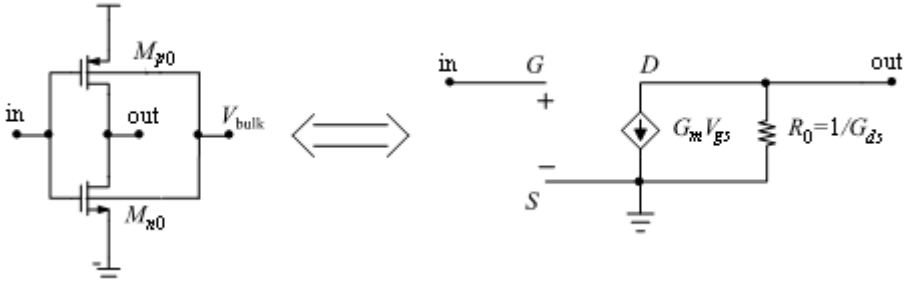

Fig. 1 – The ULV inverter and its small signal equivalent circuit.

For a large capacitive load ($C_L >> C_G$) it is accurate to assume a single-pole behaviour of the inverter, with a DC gain value of G_mR_0 and a dominant pole frequency equal to $1/(C_LR_0)$.

If the inverter is used in a diode connection (input and output shorted together), the small signal model exhibits a resistance equal to $R_0/(1+ R_0G_m)$, in

parallel with a capacitance equal to C_G. This structure may act as a load in a current-to-voltage conversion, due to the small value of the equivalent resistance; approximately equal to $1/G_m$. In the case of a k-scaled inverter, the current consumption and the small signal capacitance and conductance will be k times higher, comparing to the reference inverter. Moreover, the gain-bandwidth product will increase k times for the same load capacitance. Consequently, for our purposes, the sample inverter may be considered as a basic design element and will be used to derive all gain stages and supporting circuits for the amplifier.

In Fig. 1, the bulk terminals of the MOS transistors have been considered connected to a given voltage, V_{bulk} , since all scaled versions of the sample used in our design will have the body terminals of their devices connected to the same voltage, V_{bulk}. This voltage is properly controlled to ensure that all inverters have their trip points at half of the supply voltage. The value of this voltage is between those of the supply rails, which also ensure a reduction of threshold voltages and good circuit performances at low supply voltages.

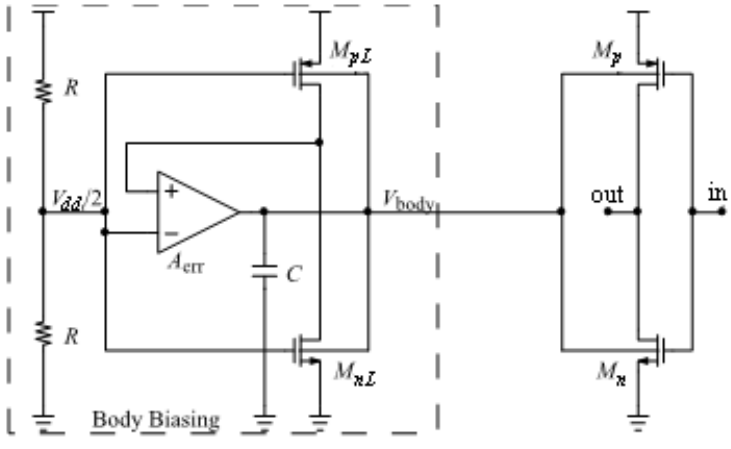

Fig. 2 – The body biasing circuit of an ULV inverter.

The body bias control circuit depicted in Fig. 2 employs a feedback loop to maintain the trip point of a scaled inverter inside the loop (M_{pL}, M_{nL}) and of any other scaled inverter (M_p, M_n) at a value equal to half of the supply voltage, using a replica bias technique. The error amplifier is built in a similar fashion as those utilized by Vieru *et al*. (2011), but with the difference that its devices have the body terminals connected to the supply rails in a standard manner. The capacitor, C, used on the output of the error amplifier, A_{err} , ensures feedback loop stability and substrate noise rejection. The error amplifier does not have drastic frequency specifications, as a good noise rejection requires for a large C, which also ensures a simple frequency compensation of the feedback loop. With

careful design, the current consumption of the body biasing circuit from Fig. 2 can be kept at a much smaller value than that of the entire circuit.

This technique offers a rail-to-rail output swing, independent of the process and temperature variations, which are very important attributes in a low-voltage environment. Unlike previous reported techniques (Tang *et al*., 2002), (Berg *et al*., 2011), our work does not make use of additional circuitry and/or special devices and has a more intuitive design approach.

2.1. ULV Scalable Inverting and Non-Inverting Current Follower

As we have seen in the previous section, a simple inverter may be used for a voltage-to-current conversion, while a diode-connected inverter may be used for a current-to-voltage conversion. Furthermore, if we cascade two identical ULV inverters, one of them being in a diode connection, we get an inverting current follower (iCF) or an inverting voltage follower (iVF).

Moreover, a cascade of two inverting followers of the same type leads to a non-inverting current or voltage follower (CF or VF), as in Figs. 3 and 4.

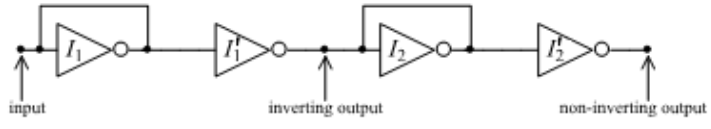

Fig. 3 – ULV inverting and non-inverting current followers.

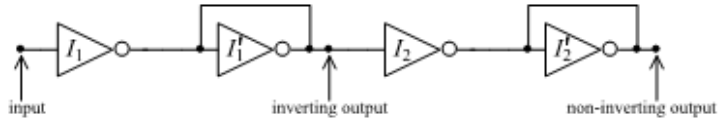

Fig. 4 – ULV inverting and non-inverting voltage followers.

The DC gains and the input/output resistances of the inverting current and voltage followers are given in the expressions

$$A_{\mathrm{iCF}} = -\left(1 - \frac{1}{1 + G_m R_0}\right) \approx -1, \quad R_{\mathrm{in_{iCF}}} = \frac{-A_{\mathrm{iCF}}}{G_m} \approx -\frac{1}{G_m}; \tag{1}$$

$$A_{\mathrm{iVF}} = -\left(1 - \frac{1}{1 + G_m R_0/2}\right) \approx -1, \quad R_{\mathrm{out_{iVF}}} = \frac{-A_{\mathrm{iVF}}}{G_m} \approx -\frac{1}{G_m}, \tag{2}$$

which may be easily used to further derive similar expressions for the non-inverting ones.

From the above expressions one may see that the performances of the inverting and non-inverting followers relate directly to those of their building inverters, so they will obey the scaling principle. Due to the sub-threshold operation of the transistors, the DC gain of the ULV inverters will be high enough to ensure that the DC gains of both inverting and non-inverting followers are close to their ideal values of –1 and +1, while their input and output resistances are close to $1/G_m$. When connected in series with capacitors, they may be used for a Reversed Nested Miller frequency compensation.

2.2. ULV Scalable Inverting Voltage Averaging Circuit

The "inverting voltage averaging circuit", from Fig. 5, uses two identical inverters acting as transconductors, and a diode-connected inverter as their common load, to ensure both the current summation and current-to-voltage conversion. If we consider that the size of the load inverter is twice the size of the input inverters, the output voltage of this circuit is approximately equal to the inverted average value of the input voltages, as in relation

$$V_{\text{out}} = -\frac{1}{2+4/G_m R_{\text{o}}}\left(V_A + V_B\right) \cong -\frac{1}{2}\left(V_A + V_B\right). \tag{3}$$

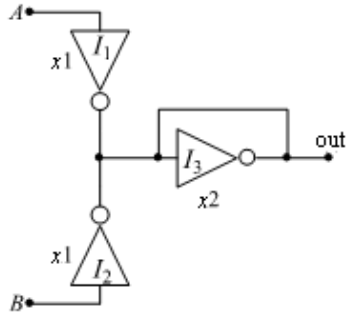

Fig. 5 – ULV inverting voltage averaging circuit.

This circuit, in conjunction with output inverters may be used to build feedforward or feedback paths for common-mode rejection of signals.

3. The Amplifier Design

Due to the ULV operation desired, it is clear that only two transistors may be stacked between power lines and cascode connections cannot be exploited to get a high DC gain. In these conditions, cascading of several simple stages seems to be the only viable option, while common-mode rejection paths and frequency compensation paths have to use very simple circuits, which require for a lot of innovative techniques.

The amplifier implemented in this work and presented in Fig. 6, is made up from three gain stages, each of them based on a pair of identical inverters: (I_{1+}, I_{1-}), (I_{2+}, I_{2-}), (I_{3+}, I_{3-}). To ensure a good common-mode rejection, each stage is accompanied by a feedforward path connected between its inputs and outputs, made from an inverting voltage averaging circuit and a pair of identical inverters as described in § **2.2.** Each path generates currents proportional to the inverted input common-mode voltage of the corresponding stage, which are used to cancel out the direct common mode output currents of that stage. For instance, in the case of the first stage, the common-mode output currents of the inverters I_{1+}, I_{1-} are cancelled by the output currents of I_{5+}, I_{5-}, as their input voltage is the output of the inverting voltage averaging circuit, I_4. The same operation is achieved in the case of the second and the third stage, where feed-forward common-mode rejection paths are respectively made from I_6, I_{7+}, I_{7-} and I_8, I_{9+}, I_{9-} .

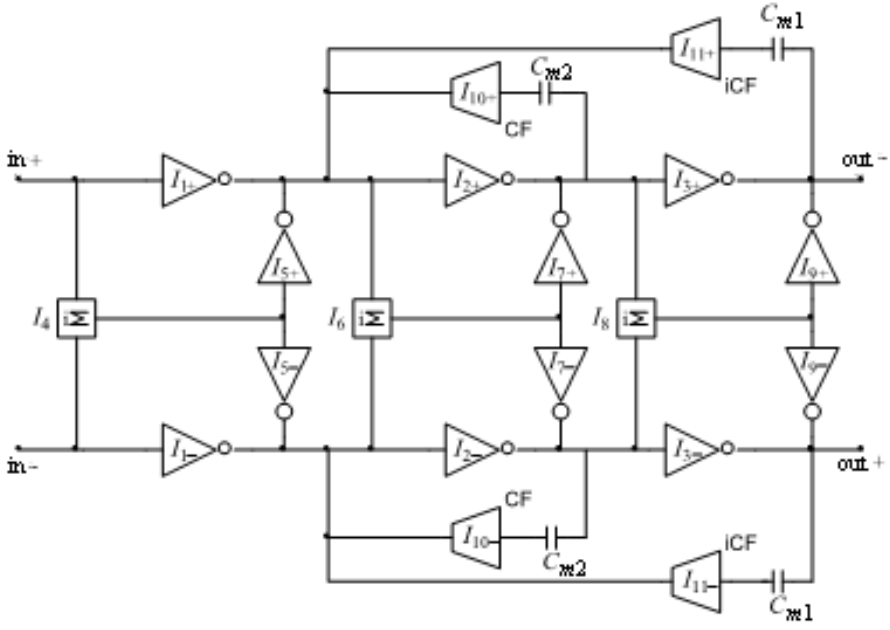

Fig. 6 – The ULV three-stage fully differential amplifier.

In essence, the differential-mode frequency compensation uses the approach utilized by Garimella *et al*. (2010). In order to employ a Reversed Nested Miller frequency compensation, balanced high-speed feedback paths have been connected from the outputs of the second and the third stage to the outputs of the first. These paths are made up from non-inverting and inverting current followers (I_{10+}, I_{10-} and I_{11+}, I_{11-}) in series with capacitors (C_{m2} and C_{m1}), in a fashion similar to that described in § **2.1**.

This technique ensures an accurate placement of the poles and zeros, which in turns allows for a good phase margin of the overall amplifier.

4. Simulation Results

The proposed amplifier was simulated for a 0.6 V supply voltage and for different temperature and process corners. The deviation with process and temperature of the output common mode voltage, around the optimum value of 0.3 V, is below 1%, which ensures a rail-to-rail operation of the amplifier over the entire temperature range (–45°C…+120°C) and for different manufacturing conditions. The differential mode frequency characteristics of the designed ULV fully-differential amplifier are shown in Fig. 7 and the main performances are summarized in Table 1, for a typical process and a nominal operating temperature (27°C). We may acknowledge that the power consumption is relatively low (P_d = 210 μW), considering the 5 MHz value of the gain-bandwidth product achieved for a 10 pF load capacitor.

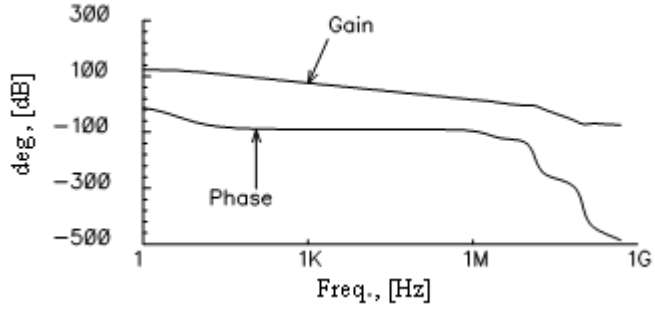

Fig. 7 – Frequency response of the amplifier.

Table 1
The Amplifier Characteristics

DC gain, [dB]	Phase margin, [°]	Gain-bandwidth, [MHz]	CMR, [dB]
127	55	5	–32

5. Conclusions

This work presents new techniques to design completely scalable ultra low voltage three-stage amplifiers, using the CMOS inverter as a basic design element. All stages are made from scaled versions of the same reference inverter, which allows for easily predictable performances and significant supply voltage reductions. The amplifier uses a body bias control circuit and feedforward paths to improve the common-mode rejection, while the frequency compensation technique is based on the Reversed Nested Miller method. This combination ensures good performances of the amplifier, over the entire temperature range and for different manufacturing conditions, when very low

supplied voltages are used. Simulation results are in good agreement with the theoretical ones, proving the validity of the proposed techniques.

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AMPLIFICATOR COMPLET DIFERENȚIAL CU TREI ETAJE PENTRU TENSIUNE FOARTE JOASĂ DE ALIMENTARE

(Rezumat)

Se prezintă o nouă abordare a construcției unui amplificator scalabil cu trei etaje, complet diferențial, pentru tensiuni foarte joase de alimentare, folosind inversorul CMOS ca unitate elementară de design. Beneficiind de avantajul unui control complet asupra ambelor tipuri de dispozitive MOS oferit de tehnologia de tip triple-well, astfel de amplificatoare pot fi proiectate pentru a funcționa la tensiuni de alimentare foarte scăzute şi cu o putere consumată redusă. Se prezintă structura completă a amplificatorului de tip rail-to-rail şi sunt discutate constrângerile de proiectare impuse de o tensiune de alimentare de 0.6 V. Circuitul a fost proiectat pentru un proces tehnologic CMOS de tip triple-well, de 0.18 μm şi este dedicat aplicațiilor care necesită un câştig ridicat de curent continuu.