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THE APPLICATION OF THE TRANSMISSION LINE PULSING TECHNIQUE ON A FULL ADDER CMOS STRUCTURE

BY

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Abstract. Recently, the studies illustrate a significant increase in the costs of the microelectronic devices, due to the failures of the devices, damaged components and loss of information. Therefore, in the process of dealing with the failures of the semiconductor devices, significant tests must be implemented. In order to observe the effects of the Electrostatic Discharge (ESD) events on CMOS structures were made several software simulations using the Transmission Line Pulse (TLP) method test. In TLP tests, the charged transmission line applies a high current pulse (simulating an ESD impulse) to the inputs of the circuits. In the paper, the test dispositive used in characterizing the ESD event, is represented by a Full Adder structure, precisely chosen due to the vulnerability of the gate transistors.

Key words: electrostatic discharge (ESD); Full Adder (FA) structure; transmission line pulse testing (TLP).

1. Introduction

Nowadays, the Electrostatic Discharge (ESD) event became a great threat to all the electronic devices due to the high vulnerability of the semiconductor devices to high voltages and currents (Vinson & Liou, 1998).

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Taking into consideration the damages caused by the ESD events on the integrated circuits, it is extremely necessary the use of an analysing process to solve the semiconductor failures. Hereby, in order to determine the damaged region, an accurate electrical model should be tested.

One of the models widely used in terms of observing and testing the electrostatic discharging events is the Transmission Line Pulse (TLP). This model allows investigating and solving ESD issues much more quickly and accurately.

Despite being a standardized model, TLP is nowadays the most preferred test method used to characterize the ESD phenomenon in semiconductor devices. The main advantage of using TLP testing consists in producing very precise, high current of square or rectangular pulses (Henry *et al*., 2000).

The commonly accepted electrostatic discharge current waveform is the one set by the IEC 61000-4-2 standard. The corresponding waveform of the TLP test method will differ from the waveforms of the standardized ESD models (Barth *et al*., 2001). In the case of TLP tests are implemented square waveforms with controlled amplitude and time length (Hyatt *et al*., 2001). The characteristic waveform of the TLP test illustrates the basic failure mechanisms of the integrated circuits due to the ESD phenomenon. In the TLP tests a charged transmission line is usually used to apply high currents to the integrated circuits.

In terms of failure, the MOS field-effect transistors (MOSFET) have been reported with poor ESD reliability (Chen & Ker, 2003). Due to the low breakdown voltage of the gate oxide in CMOS structures, high-performance designs demand a good understanding of the proximity effects on the implemented circuits (effects that arise as results of the increase of the leakage current at the inputs of CMOS circuits). In order to observe these proximity effects on the CMOS structures, should be taken into consideration effective tests.

To systematically characterize the novice effects of the ESD discharges, in the paper were summarized the TLP tests made on a CMOS structure (the structure considered: the one-bit Full Adder), through circuit modeling and simulation.

2. Design Considerations of a Full Adder Structure

For the past years, in digital applications, innovative Full Adder (FA) designs have captured the interest of designers. An FA can be implemented in many different ways. In Fig. 1 is illustrated the corresponding symbol of the one-bit FA CMOS structure.

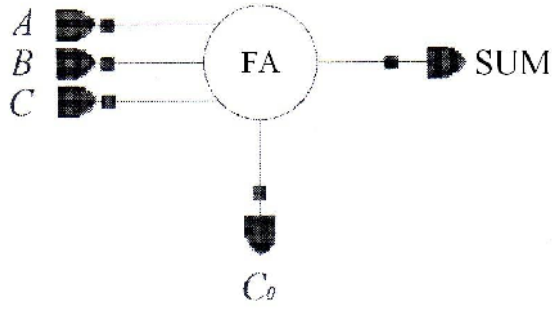

Fig. 1 – The corresponding symbol of the Full Adder CMOS structure.

The equivalent schematic of the FA is represented in Fig. 2. The conventional CMOS FA (Fig. 2) was implemented in a 0.35 μm CMOS technology, using a number of 24 transistors and two inverters.

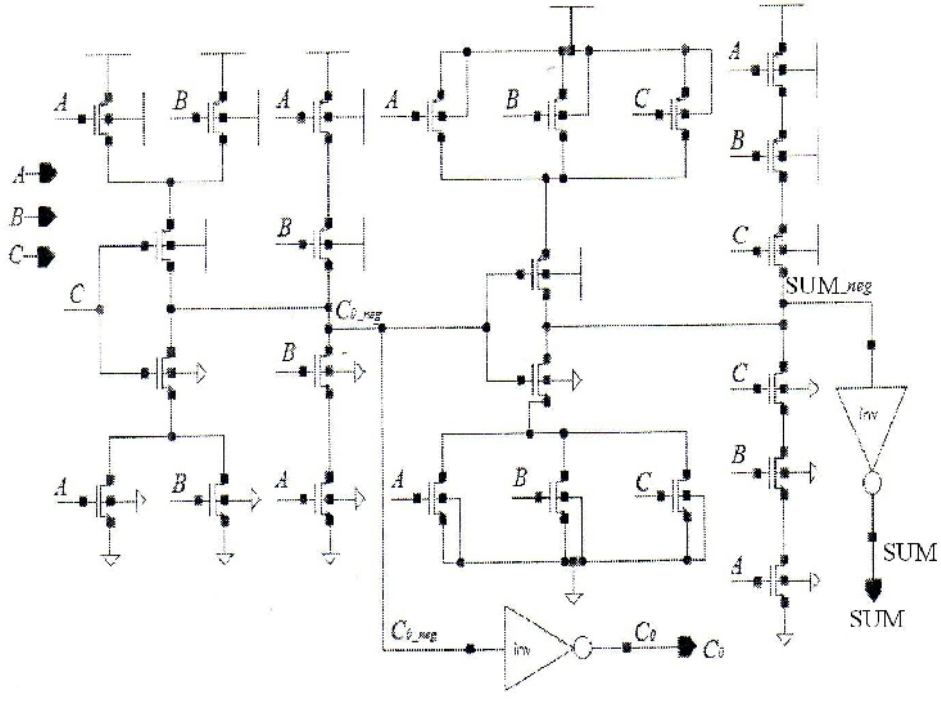

Fig. 2 – The conventional configuration of the Full Adder CMOS cell.

3. Transmission Line Pulse Testing of the One-Bit Full Adder Structure

3.1 Typical Transmission Line Pulse

The TLP is a model widely used in the test field for analysing the behavior of a device, when it is exposed to an ESD event (Voldman *et al*., 1999). Despite not being a standardized model, TLP is, nowadays, the most used test method for characterizing the ESD events in semiconductors devices.

The TLP test technique provides a number of pulses with controlled amplitude and time length (having a specific energy), generating square waveforms. In the process of TLP testing, a high voltage source charges the transmission line to a certain voltage which further is discharged into the pins of the test device (device under test – DUT), resulting in a square current pulse applied on the device (Fig. 3).

In Figs. 3 and 4 are illustrated the representative schematic and the characteristic waveform of the TLP test.

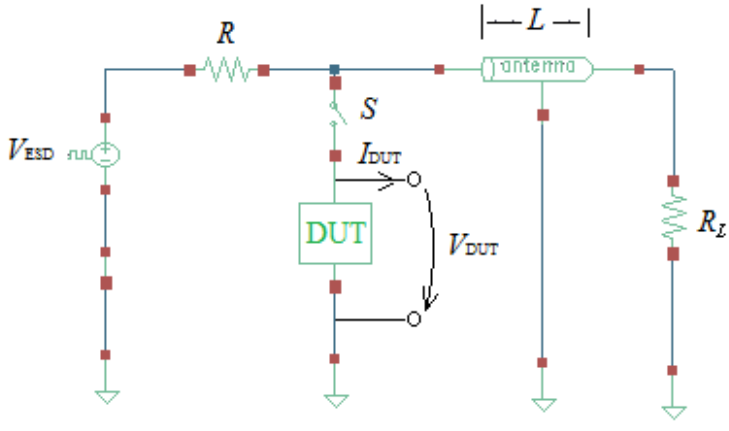

Fig. 3 – The schematic of the Transmission Line Pulse model.

The high voltage source controls the waveform amplitude, while the pulse duration is set by the time delay (determined by the transmission line length) (Fig. 4). The V_{ESD} voltage charges the L transmission line of 10 m length and 100 ns pulse width, through resistor R. From the high voltage source to the DUT, the system has constant impedance, (the characteristic impedance of the line, Z_0= 50 Ω).

In the ESD tests, the use of the charged transmission line is similar to the use of a charged capacitor.

Knowing that TLP model is mainly used in the characterization of the semiconductor devices, in what follows these tests will be applied to a CMOS

structure, with vulnerable and thin gate oxides. Therefore, if initially for the test dispositive, (DUT), was considered a resistance of 1 Ω, further, the resistance will be replaced with the FA structure.

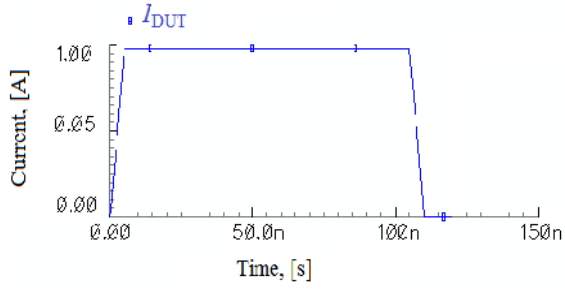

Fig. 4 – The characteristic waveform of the Transmission Line Pulse model.

3.2. Transmission Line Pulse Testing Using a Full Adder Structure

In this paper, TLP test technique was precisely chosen because of its ability of understanding the semiconductor device response to the high current pulses. In Fig. 5, the high voltage source delivers enough power to stress the *A* input of the FA structure.

The tests made were realized using a smaller transmission line of 8 m length, having 80 ns pulse width and 800 ps fast time rise.

In the representation of the block diagram from Fig. 5, the transition time of the *S* switch (open–close) is about 1 ns. Initially, the static electricity is stored in the transmission line through resistor *R*. When the switch changes its state, the transmission line discharges on the input of the test dispositive (in our case: *A* input of the FA).

Taking into consideration the short transition time of the switch and the voltage signal of 1 kV, the effects of the discharging process will cause an extra stress to the testing device. Therefore, in order to observe these effects, the simulation of the circuit represented in Fig. 5 was realized for a period of 200 ns, having a 50 ns step. The step was chosen in terms of increasing the accuracy of the waveform display.

The waveforms of the tests applied on the FA structure, using TLP are illustrated in Fig. 6. The simulations are made for the case of applying a high voltage pulse to one input of the FA structure (input *A*).

From the obtained results using TLP testing, we observe the device degradation of the *A* input waveform of the FA. The high impulse from the charged transmission line applied on the FA transistors gate determines the breakdown of the semiconductor junctions. In these conditions will result the malfunction of the entire circuit. Therefore, in order to avoid the breakdown event is necessary to use optimal protection device.

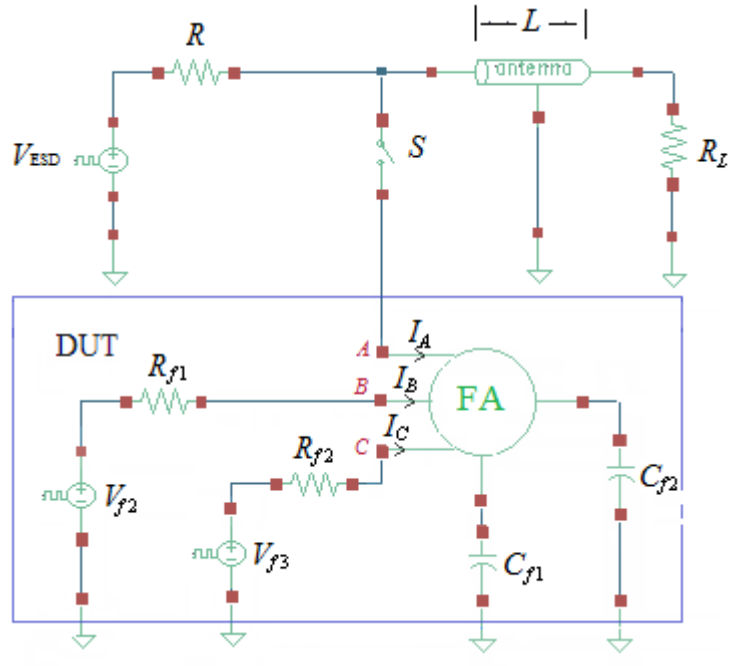

Fig. 5 – The characteristic circuit of the Transmission Line Pulse testing a Full Adder CMOS structure.

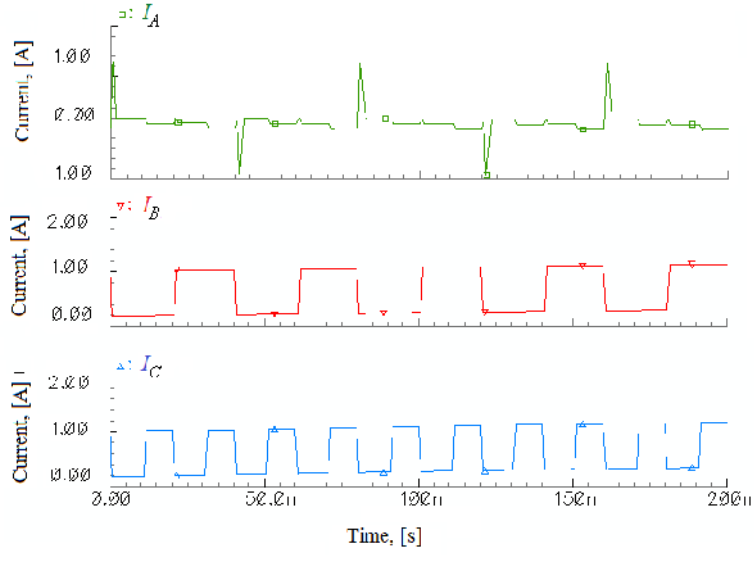

Fig. 6 – The simulated waveforms of the Transmission Line Pulse testing using a Full Adder CMOS structure.

Knowing that the spectrum of constraints regarding ESD discharges is quite broad, it is quite impossible to achieve immunity to ESD. However, using adequate protection can improve the reliability of the semiconductors.

The implemented tests have a big importance in determining the susceptibility level to ESD events and evaluating the necessity of the protection circuitry for semiconductor devices. Hereby, the tests implemented are extremely useful for future applications and represent the background in the investigation of the innovative protection structures for semiconductor devices.

4. Conclusions

The paper is focused on the description of the TLP test technique in analysing the behavior of the one-bit FA structure, on applying at one input a high ESD current pulse. The simulation using TLP test method is extremely important in order to observe the effects and the damage of the ESD discharges on the vulnerable gate transistors. Observing the serious damages of the devices, accordingly with ESD effects, protective structures are demanded. Therefore, the performed tests will be used in a further work in order to determine optimal protective circuits.

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METODĂ DE TESTARE LA DESCĂRCĂRI ELECTROSTATICE A TRANSMISIEI LINIILOR PULSATORII ASUPRA CIRCUITULUI SUMATOR ÎN TEHNOLOGIE CMOS

(Rezumat)

Recent, studiile relevă o creştere semnificativă a costurilor dispozitivelor microelectronice, datorită defectelor numeroase observabile în dispozitive, componentelor deteriorate şi pierderii informației. Aşadar, în scopul reducerii apariției acestor defecte sunt necesare teste de specialitate, care să simuleze cu exactitate evenimentele de descărcare electrostatică. În vederea asigurării unor teste fiabile de descărcări electrostatice în cazul circuitelor CMOS, s-au realizat un număr de simulări software utilizând ca metodă de testare, Transmisia Liniilor Pulsatorii (TLP).

Procedeul de testare TLP constă în încărcarea unei linii de transmisie şi aplicarea unui curent de dimensiuni mari la una din intrările circuitului de testare. În lucrare, dispozitivul de testare utilizat pentru caracterizarea unui eveniment DES este reprezentat printr-un circuit de sumare, structură considerată în mare parte datorită vulnerabilității tranzistoarelor aflate în componența schemei de circuit. Rolul testelor implementate a constat în determinarea impactului curenților de dimensiuni ridicate asupra semiconductoarelor.