BULETINUL INSTITUTULUI POLITEHNIC DIN IAŞI
Publicat de
Universitatea Tehnică „Gheorghe Asachi” din Iaşi
Tomul LVIII (LXII), Fasc. 3, 2012
Secţia
ELECTROTEHNICĂ. ENERGETICĂ. ELECTRONICĂ

NEW APPROACH FOR PLL LOOP FILTER DESIGN USING LINEAR PROGRAMMING AND SEMI-DEFINITE PROGRAMMING

BY

HALA J. EL-KHOZONDAR*, AYMAN ALQOQA and HATEM ELAYDI

Islamic University of Gaza, Palestine
Electrical Engineering Department

Received: September 12, 2012
Accepted for publication: October 31, 2012

Abstract. Achieving optimal design of phase-locked loop (PLL) is a major challenge in WiMax technology in order to improve system behaviour (overshoot & settling time). A new loop filter design method for PLLs is introduced taking into consideration various mobile WiMax design objectives namely: small settling time, minimum overshoot and working mobile WiMax frequency range. Filter design based on optimizing conflicting objectives is accomplished *via* linear programming and Semi-Definite Programming (SDP) in conjunction with appropriate adjustment of certain design parameters. Digital Finite Impulse Response (FIR) filter is designed using linear programming and SDP shows better results than other comparable designs. The filter design based on SDP outperformed the design based on Linear Programming.

Key words: Semi-Definite Programming; Linear Programming; Mobile WiMax; Frequency Synthesizer; Phase Locked Loop; FIR Filter Design.

1. Introduction

Worldwide Interoperability for Microwave Access (WiMax) lays the foundation for the fourth generation (4G) of mobile broadband networks (2010). WiMax Quality of Service (QoS) guaranteed for different traffic classes, robust

*Corresponding author: *e-mail*: hkhozondar@iugaza.edu.ps

security, and mobility. The phase-locked loop (PLL) is an electronic circuit that controls an oscillator in order to maintain a constant phase angle relative to a reference signal (Digital PLL, 2010), plays a significant part in WiMax system. One of the most common uses of a PLL is in frequency synthesizers of wireless systems. A frequency synthesizer generates a range of output frequencies from a single stable reference frequency of a crystal oscillator (Best, 2007). Many applications in communication require a range of frequencies or a multiplication of a periodic signal. For example, in most of the FM radios, a phase-locked loop frequency synthesizer technique is used to generate 101 different frequencies. Also most of the wireless transceiver designs employ a frequency synthesizer to generate highly accurate frequencies, varying in precise steps, such as from 600 MHz to 800 MHz in steps of 200 kHz. Frequency Synthesizers are also widely used in signal generators and in instrumentation systems, such as spectrum analysers and modulation analysers. A basic configuration of a frequency synthesizer is shown in Fig. 1.

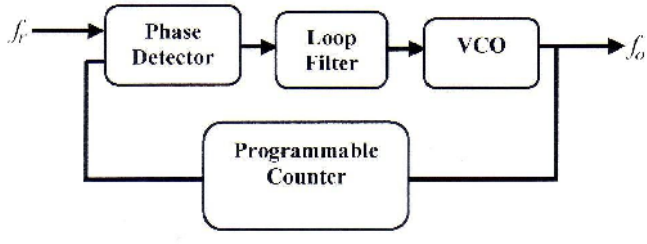

Fig. 1 – Basic Frequency Synthesizer.

Besides a PLL, it also includes a very stable crystal oscillator and *N*-programmable divider in the feedback loop. The programmable divider divides the output of the Voltage Controlled Oscillator (VCO) by *N* and locks to the reference frequency generated by a crystal oscillator.

The output frequency of VCO is a function of the control voltage generated by the phase detector/comparator (PD). The output of the phase comparator, which is proportional to the phase difference between the signals applied at its two inputs, controls the frequency of the VCO. So the phase comparator input from the VCO through the programmable divider remains in phase with the reference input of crystal oscillator. Thus, the VCO frequency is maintained at Nf_r. This relation can be expressed as

$$f_r = \frac{f_o}{N}, \tag{1}$$

where f_r is fractional frequency and N is an integer number. This implies that the output frequency is equal to

$$\theta_o = \frac{G(s)}{1 + G(s)H(s)}\theta_i(s). \tag{2}$$

Using this technique one can produce a number of frequencies separated by f_r and a multiple of N. For example, if the input frequency is 24 kHz and the N is selected to be 32 (a single integer) then the output frequency will be 0.768 MHz. In the same way, if N is a range of numbers, then output frequencies will be in the proportional range. This basic technique can be used to develop a frequency synthesizer from a single reference frequency. This is the most basic form of a frequency synthesizer using phase locked loop technique. As in Fig. 1, $\theta_i(s)$ represents the phase input, $\theta_e(s)$ the phase error, and $\theta_o(s)$, the output phase. Phase error (phase detector output) can be calculated such as

$$\theta_e = \frac{1}{1+G(s)H(s)}\theta_i(s), \tag{3}$$

and the VCO output can be calculated such as

$$\theta_o = \frac{G(s)}{1+G(s)H(s)}\theta_i(s), \tag{4}$$

where $G(s)$ is the product of the individual feed forward transfer functions, and $H(s)$ – the product of the individual feedback transfer functions (Best, 2007).

The filtering operation of the error voltage (coming out from the PD) is performed by the loop filter. The output of PD consists of a dc component superimposed with an ac component. The ac part is undesired as an input to the VCO, hence a low pass filter is used to filter out ac component. Loop filter is one of the most important functional blocks in determining the performance of the loop. In addition, a loop filter introduced poles to the PLL transfer function, which, in turn, is a parameter in determining the bandwidth of the PLL. Since higher order loop filters offer better noise cancelation, a loop filter of order 2 or more are used in most of the critical application PLL circuits.

The main contribution of this paper is designing PLL loop filter that meets certain specifications and works properly and efficiently with Mobile WiMax system. Selecting the filter's coefficients is based on LP and SDP optimization techniques. The problem is to design and optimize PLL loop filter using SDP optimization that is compatible with Mobile WiMax system. The designed loop filter must be stable and meet the following specifications:

a) Frequency range: 2.3…2.7 GHz used for Mobile WiMax systems.

b) Small settling time, to lower the lock-in range.

c) Very small overshoot.

One desirable property of all PLLs is that the reference and feedback clock edges be brought into very close alignment. The average difference in time between the phases of the two signals, when the PLL has achieved lock, is called *the static phase offset* (also called the steady-state phase error). The variance between these phases is called *tracking jitter*. Ideally, the static phase offset should be zero, and the tracking jitter should be as low as possible.

Phase noise is another type of jitter observed in PLLs, and is caused by

the oscillator itself and by elements used in the oscillator's frequency control circuit. Some technologies are known to perform better than others in this regard. The best digital PLLs are constructed with emitter-coupled logic (ECL) elements, at the expense of high power consumption. To keep phase noise low in PLL circuits, it is best to avoid saturating logic families such as transistor–transistor logic (TTL) or CMOS.

Traditional frequency synthesizers use low-pass analog filter to eliminate the high frequency components, but in this paper we use FIR digital low-pass filter to eliminate the high frequency components in order to improve noise immunity. *N*-Fractional Synthesizer is used instead of *N*-Integer Synthesizer to reduce noise resulted from the factor *N*.

This paper is organized as follows: section **2** covers methodology used to design and optimize PLL loop filter. FIR low-pass digital filter using LP and SDP methods is introduced in section **3**. Section **4** shows the results and discussions of LP and SDP designs. Conclusion and future work are outlined in section **5**.

2. Methodology

The fractional-*N* PLL block diagram shown in Fig. 2 consists of

a) Phase/Frequency detector which is assumed XOR type.

b) Loop Filter which is the objective of our design which is a Low-Pass Filter (LPF).

c) Voltage Control Oscillator (VCO).

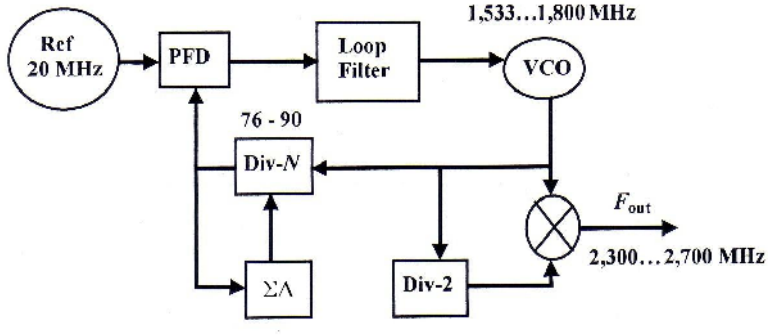

Fig. 2 – Fractional-*N* PLL block diagram.

We started by designing an Integer-*N* PLL: 125 kHz reference pushes *N* from 18,400 to 21,600 (2,700/.125). The resulted loop filter cutoff (< 12.5 kHz) produced big settling time and the VCO phase noise increased by $20 \log_{10}(N) \approx$ ≈ 87 dB.

To overcome the previous drawback, we used Multi-Modulus Fractional PLL with the following specifications:

a) Fractional value between *N* and $2N - 1$ (64-127).

b) Sigma Delta Modulator (Programmable resolution).

c) Large Reference (20 MHz) for good tradeoff with settling time.

d) Reduced N impact on phase noise by 45 dB over Integer N.

E x a m p l e. To obtain 2,300 MHz frequency, we produced 1,533 MHz (from VCO) and then upconvert it to 2,300 MHz (1,533 MHz × × 1.5 ≈ 2,300 MHz). The 1,533 MHz can be produced with $N = 76$ and a fraction equal to 0.65 (means that 20 MHz × (76 + 0.65) = 1,533 MHz).

As a result, for $N = (76...90)$, it can produce a frequency range (1,533 MHz ... 1,800 MHz), which can be upconverted to (2,300 MHz ... 2,700 MHz).

Fig. 2 shows the Fractional-N PLL design block diagram, with N range from 76 to 90; $\Sigma\Delta$ is the fraction. Our goal now is to design digital FIR low pass loop filter in order to meet the previously mentioned requirements. The design will be encouraged by two different optimization methods, LP and SDP.

3. FIR Low-Pass Filter Design Theory

We consider the problem of designing a finite impulse response (FIR) filter with upper and lower bounds on its frequency response magnitude (Wu *et al*., 1996): given filter length N, find filter tap coefficients $h \in \mathbb{R}^N$, $h = (h(0), ..., h(N-1))$, such that the frequency response $H(\omega) = \sum_{i=0}^{N-1} h(n)\mathrm{e}^{-\mathrm{j}\omega n}$ satisfies the magnitude bounds

$$L(\omega) \le |H(\omega)| \le U(w),\ \omega \in \quad \subseteq [\quad] \tag{5}$$

over the frequency range, Ω, of interest.

One conventional approach to FIR filter design is Chebychev approximation of a desired filter response, $D(\omega)$, *i.e*., one minimizes the maximum approximation error over Ω.

We present a new way of solving the proposed class of FIR filter design problems, based on magnitude design, *i.e*., instead of designing the frequency response $H(\omega)$ of the filter, directly, we design its power spectrum, $|H(\omega)|^2$, to satisfy the magnitude bounds (Wu *et al*., 1996).

Let autocorrelation function, $r(n)$, denote

$$r(n) = \sum_{k=-\infty}^{\infty} h(k)h(k+n), \tag{6}$$

where we take $h(k) = 0$ for $k < 0$ or $k > N - 1$. The sequence $r(n)$ is symmetric around $n = 0$, zero for $n \le -N$, and $r(0) \ge 0$. Note that the Fourier transform of $r(n)$

$$R(\omega) = \sum_{n=-\infty}^{\infty} r(n) \mathrm{e}^{-\mathrm{j}\omega n} = \left| H(\omega) \right|^2,$$

is the power spectrum of $h(n)$. If we use r as our design variables, we can reformulate the FIR design problem in $\mathbb{R}^N$ as

$$\begin{aligned} \text{find} \quad & r = \left(r(0), \ldots..., r(N-1) \right), \\ \text{subject to} \quad & L^2(\omega) \le R(\omega) \le U^2(\omega), \ \omega \in \\ & R(\omega) \ge 0, \ \omega \in [0, \pi]. \end{aligned} \tag{7}$$

The non-negativity constraint $R(\omega) \ge 0$ is a necessary and sufficient condition for the existence of x satisfying (6) by the Fejér-Riesz theorem (s. § **4** in the paper published by Wu *et al*., (1996)). Once a solution of (7) is found, an FIR filter can be obtained *via* spectral factorization. An efficient method of minimum-phase spectral factorization is given in Section **4** by Wu *et al*., 1996.

3.1. LP Formulation

A common practice of relaxing the semi-definite program (7) is to solve a discretized version of it, *i.e.,* impose the constraints only on a finite subset of the $[0, \pi]$ interval and the problem becomes

$$\begin{aligned} \text{find} \quad & r = \left(r(0), \ldots..., r(N-1) \right), \\ \text{subject to} \quad & L^2(\omega_i) \le R(\omega_i) \le U^2(\omega_i), \ \omega_i \in \\ & R(\omega_i) \ge 0, (i = 1, ..., M), \end{aligned} \tag{8}$$

where $0 \le \omega_1 < \omega_2 < \ldots < \omega_M \le \pi$. Since $R(\omega_i)$ is a linear function in r for each i, (8) is in fact a linear programming problem that can be efficiently solved. When M is sufficiently large, the LP formulation gives very good approximations of (7). A rule of thumb of choosing M, $M \approx 15N$, is recommended by Alkhairy *et al*., (1998). According to that we assumed $M = 15N$ along this paper.

3.2. SDP Formulation

We will show that the non-negativity of $R(\omega_i)$ for all $\omega \in [0, \pi]$ can be cast as an LMI (Boyd *et al*., 1994) constraint and imposed exactly at the cost of $N(N-1)/2$ auxiliary variables. We will use the following

T h e o r e m 1. *Given a discrete-time linear system* (A, B, C, D), *A stable*, (A, B, C) *minimal and* $D + D^T \ge 0$, *the transfer function* $H(z) = C(zI - A)^{-1}B + D$ *satisfies relation*

$$H\left(\mathrm{e}^{\mathrm{j}\omega}\right)+H^{*}\left(\mathrm{e}^{\mathrm{j}\omega}\right)\geq 0 \quad \textit{for all} \quad \omega\in[0,2\pi]$$

if and only if there exists real symmetric matrix P such that the matrix inequality

$$\begin{bmatrix} P-A^{T}PA & C^{T}-A^{T}PB \\ C-B^{T}PA & D+D^{T}-B^{T}PB \end{bmatrix}\geq 0 \tag{9}$$

is satisfied. Detailed proof of this theorem can be found in a paper published by Wu *et al*., (1996).

In order to apply Theorem 1, we would like to define $H(z)$ as deadbeat, system where $H(z)$ is defined as a rational function, its denumerator consisting of one term with z to the power of N. Then, this system is represented in delay mode, z^{-1}, which leads to a polynomial with N coefficients stored in array r. Thus, (A, B, C, D) is defined such as

$$H\left(z\right)=C(zI-A)^{-1}B+D=\frac{1}{2}r\left(0\right)+r\left(1\right)z^{-1}+\cdots+r\left(N-1\right)z^{-\left(N-1\right)}. \tag{10}$$

An obvious choice is the controllability canonical form

$$A=\begin{bmatrix} 0 & 0 & \cdots & 0 \\ 1 & 0 & \cdots & 0 \\ & 1 & & \\ \vdots & & \ddots\ \ddots & \vdots \\ 0 & & 1 & 0 \end{bmatrix},\ B=\begin{bmatrix} 1 \\ 0 \\ \vdots \\ 0 \end{bmatrix}, \tag{11}$$

$$C=\begin{bmatrix} r(1) & r(2) & \cdots & r(N-1) \end{bmatrix},\quad D=\frac{1}{2}r(0).$$

It can be easily checked that (A, B, C, D) given by (11) satisfies (10) and all the hypotheses of Theorem 1. Therefore the existence of r and symmetric P that satisfy the matrix inequality (9) is the necessary and sufficient condition for $R(\omega)$ for all $\omega\in[0,\pi]$ by Theorem 1.

Note that (9) depends affinely on r and P. Thus we can formulate the SDP feasibility problem

$$\begin{aligned} &\text{find} \quad r\in\mathbb{R}^{N} \text{ and } P=P^{T}\in\mathbb{R}^{N-1\times N-1}\left(r\left(0\right),\ldots..,r\left(\acute{N}-1\right)\right), \\ &\text{subject to} \quad L^{2}\left(\omega_{i}\right)\leq R\left(\omega_{i}\right)\leq U^{2}\left(\omega_{i}\right),\ \omega_{i}\in \\ &\begin{bmatrix} P-A^{T}PA & C^{T}-A^{T}PB \\ C-B^{T}PA & D+D^{T}-B^{T}PB \end{bmatrix}\geq 0, \end{aligned} \tag{12}$$

with (*A*, *B*, *C*, *D*) given by (11). The SDP feasibility problem (12) can be cast as an ordinary SDP and solved efficiently.

4. Results and Discussions

In order to perform simulation for the designed filters, a simulation module as shown in Fig. 3 is built using MATLAB and Simulink.

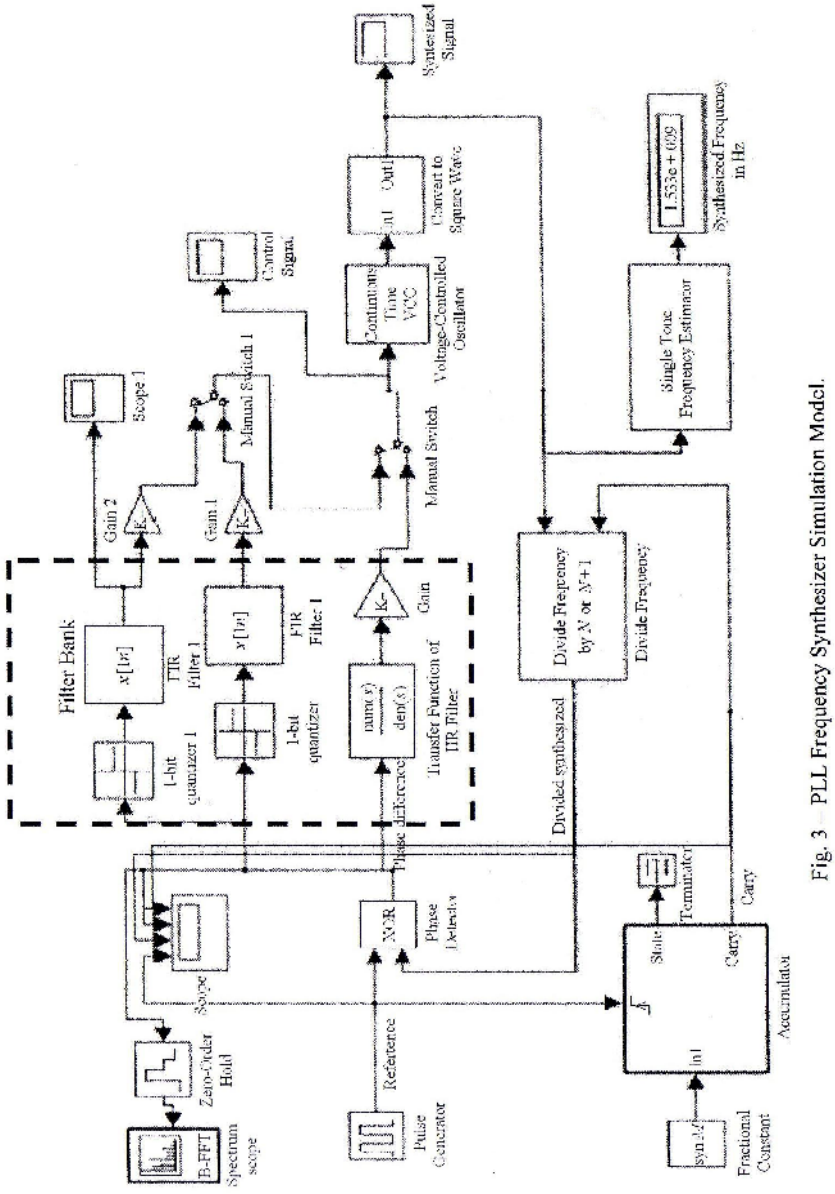

Fig. 3 PLL Frequency Synthesizer Simulation Model.

The FIR filters parameters are obtained using the MATLAB convex optimization toolbox, CVX (2009). The simulation module consists of

a) *Reference Frequency*: pulse generator is chosen to produce 20 MHz.

b) *Filter Bank*: two filters are designed and separated by manual switch as shown in Fig. 3.

c) *Voltage Controlled Oscillator* (*VCO*), with output signal amplitude equal to 1 V, quiescent frequency equal to 1.511 GHz, and input sensitivity equal to 10 MHz/V.

d) *Phase Detector*: XOR type selected.

e) *Frequency Divider* which produces (syn N + syn M) values used to divide the output of VCO, where syn N is the integer and syn M is the fraction.

f) *Sigma/Delta Modulator*: to produce the required fraction syn M.

g) The *Gain formula*

$$K = K_x \frac{(\text{syn } Fr \ \text{syn } N - \text{syn } Fq)}{\text{syn } Sen},$$

where $K_x = 2.5$ after the output of FIR filter.

The simulation model produced synthesized frequency in the range of (1.533 GHz…1.8 GHz) that must be multiplied by 1.5 to obtain the required range (2.3 GHz…2.7 GHz).

4.1. Linear Programming

The FIR filter design is obtained using LP as shown in Fig. 4.

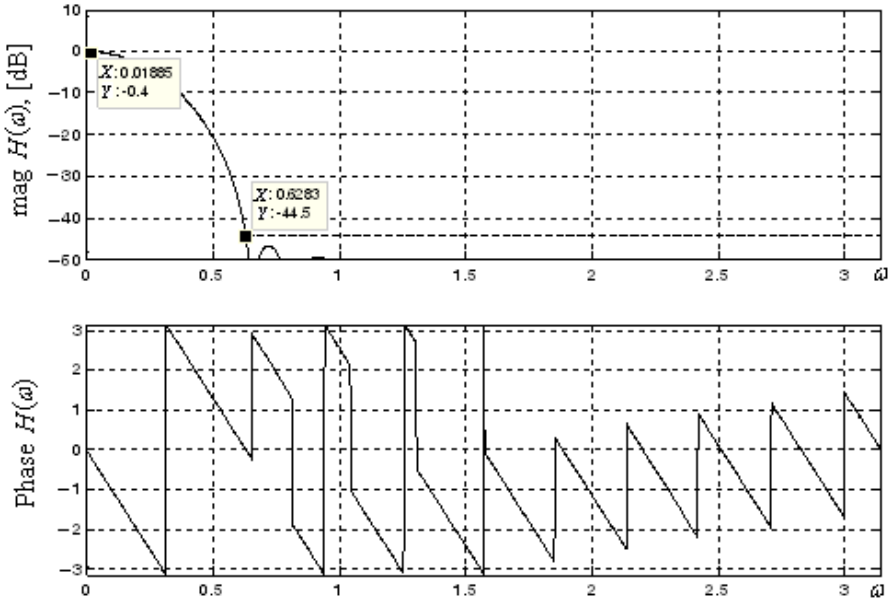

Fig. 4 – Magnitude/Phase Response (LP).

Fig. 4 shows the designed FIR filter length of 21 taps where filter order equals to 20. This figure shows that

a) The maximum passband ripple does not exceed 0.4 dB with ω_{pass} = = 0.01885 = 0.006π rad/s.

b) Stopband attenuation is below –44.5 dB with ω_{stop} = 0.6283 = = 0.2π rad/s.

The simulation results of the Mobile WiMax for this FIR filter produced the correct and proper output frequency as shown in Fig. 3. The simulation result of the control signal using this FIR filter as shown in Fig. 5 produced zero overshoot, rise time of 0.2749 μs and settling time of 0.5498 μs.

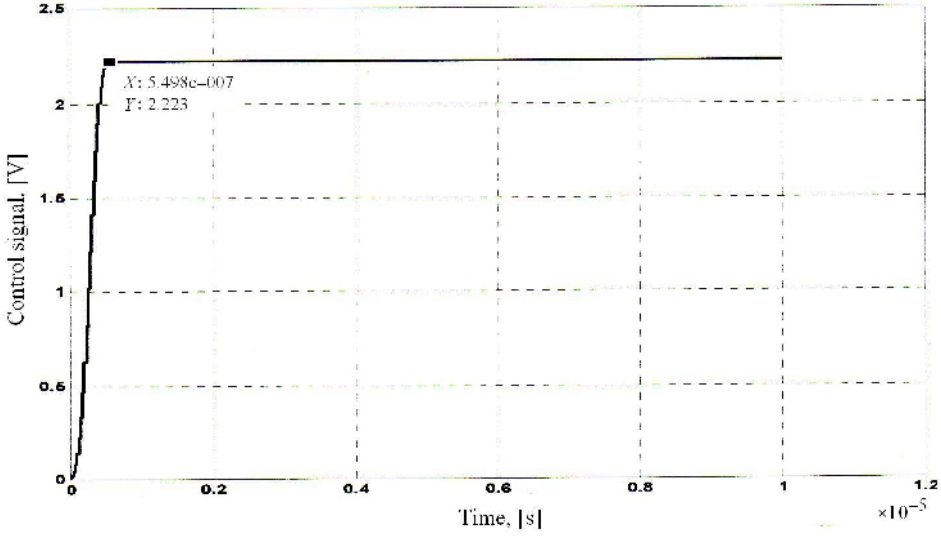

Fig. 5 – Control Signal of VCO input using Designed FIR Filter.

4.2. SDP

The second FIR filter design is obtained using SDP as shown in Fig. 6.

Fig. 6 shows a 19 taps FIR filter with filter order of 18 (fewer than LP FIR length). This figure shows that

a) The maximum passband ripple does not exceed 0.4 dB with ω_{pass} = = 0.01885 = 0.006π rad/s.

b) Stopband attenuation is below –44.5 dB with ω_{stop} = 0.6283 = = 0.2π rad/s.

The simulation results of Mobile WiMax as shown in Fig. 3 worked properly and produced the correct output frequency. The simulation results of the control signal using this FIR filter as shown in Fig. 7 produced: zero overshoot, rise time of 0.25 μs, a settling time of 0. 4998 μs.

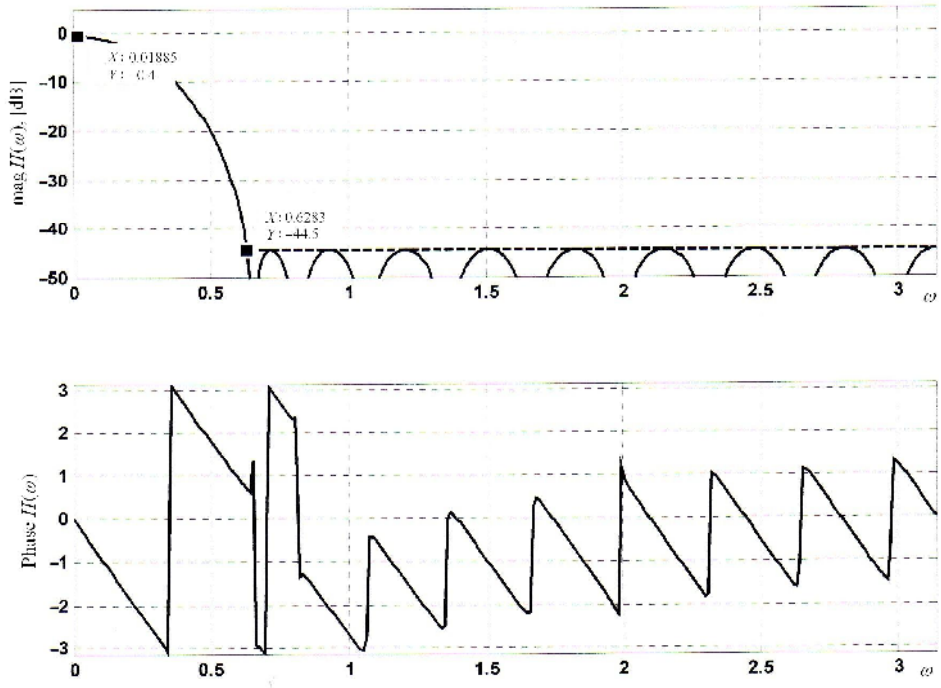

Fig. 6 – FIR Filter Magnitude/Phase Response (SDP).

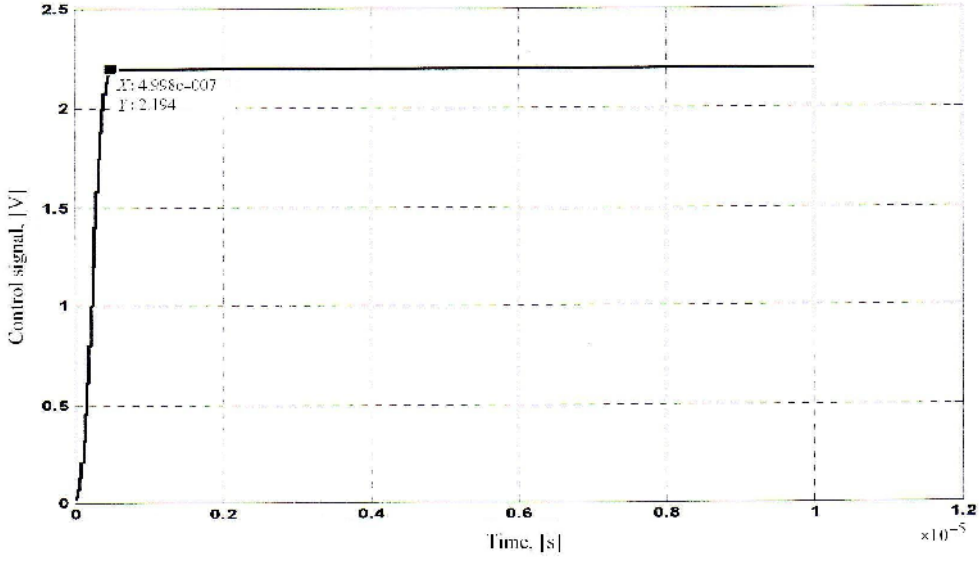

Fig. 7 – Control Signal of VCO input using Designed FIR Filter (SDP).

The filter design using SDP technique outperformed LP technique with reduced filter length of 19 taps instead of 21 taps, lower settling time and lower rise time. Moreover, the proposed SDP filter design also outperformed filter designs by Chou *et al*. (2006), Staggs (2009) and Kozak & Friedman (2004) in terms of settling time and overshoot as shown in Table 1. Unfortunately, the rise time did not meet Chou's and Staggs' results. Filter design using SDP outperformed other techniques regarding filter order, settling time and overshoot.

Table 1
Comparison between Proposed FIR Digital Filter Designs and Other Designs

	FIR filter design (LP), [μs]	FIR filter design (SDP) , [μs]	Chou, [μs]	Staggs, [μs]	Kozak, [μs]
Settling time	0.5498	0.4998	40	40	≈ 10
Rise time	≈ 0.2749	≈ 0.25	≈ 0.07313	≈ 0.1	≈ 1
Overshoot	Zero	Zero	≈ 21%	≈ 25%	≈ 29.6%

5. Conclusions and Future Work

Achieving optimal design of phase-locked loop in WiMax technology in order to improve system behavior (overshoot & settling time) is a current research field. A new loop filter design method for frequency synthesizer used in mobile WiMax was proposed taking into consideration various design objectives: small settling time, minimum overshoot and mobile WiMax frequency range. FIR digital low pass filter was designed using linear programming and semi-definite programming. Simulations results showed that FIR lowpass digital filter utilizing linear programming and semidefinite programming managed to improve the transient behavior. The simulated results showed that the filter met the Mobile WiMax systems working frequency range of 2.300 GHz…2.700 GHz; however, it can be extended to include much higher frequency bands. The SDP designed outperform the LP filter design and did much better than similar work by others. Further research can concentrate more on VCO noise and optimizing filter order.

REFERENCES

Alkhairy A., Christian K., Lim J., *Design of FIR Filters by Complex Chebyshev Approximation*. Proc. of the Acoustics, Speech a. Signal Proc., Washington, DC, USA, 1991, 1985-1988.

Best R.E., *Phase-Locked Loops: Design, Simulation, and Applications*. Sixth Ed., McGraw Hill, NY, 2007.

Boyd S., El Ghaoui L., Feron E., Balakrishnan V., *Linear Matrix Inequalities in System and Control Theory*. SIAM, Philadelphia, 1994.

Chou Y., Mao W., Chen Y., Chang F., *A Novel Loop Filter Design for Phase-Locked Loops*. The Internat. IEEE Conf. on Syst., 2006, 2932-2938.

Kozak M., Friedman E., *Design and Simulation of Fractional-N PLL Frequency Synthesizers*. Proc. of the 2004 Internat. Symp. on Circ. a. Syst., 2004, IV-780-3.

Wu S.-P., Boyd S., Vandenberghe L., *FIR Filter Design Via Semidefinite Programming and Spectral Factorization*. The 35th IEEE Decision and Control Conf., 1996, 271-276.

* * * *CVX, MatLab Software for Disciplined Convex Programming*. Availiable at: http://www. stanford.edu/~boyd/cvx/, (accessed Oct. 15, 2009).

* * * Digital PLL, Univ. of Aberdeen, Availiable at:http://www.erg.abdn.ac.uk/users/ gorry/course/phy-pages/dpll.html, (accessed Jan. 10, 2010).

* * * *Staggs Ansoft, Mobile WiMax Radio Phase Locked Loop Design*. Availiable at: http://www. ansoft.com/converge/staggs_ansoft.pdf, (accessed March 15, 2009).

* * * Wikipedia.Availiable at:http://en.wikipedia.org/wiki/Phase-locked_loop, (accessed Feb. 15, 2011).

* * * WiMax Forum; Availiable at: http://www.wimaxforum.org/home, (accessed Feb 15, 2010).

O ABORDARE NOUĂ A PROIECTĂRII FILTRELOR DIN BUCLA PLL UTILIZÂND PROGRAMAREA LINIARĂ ŞI SEMI-DEFINITĂ

(Rezumat)

Realizarea proiectării optime a buclelor de calare a fazei (PLL) constituie o provocare majoră în tehnologia WiMax în scopul de a îmbunătăți comportarea sistemului (supracreştere şi timp de stabilizare). Se propune o nouă metodă de proiectare a filtrelor pentru PLL, care ia în considerare diversele obiective de proiectare din sistemele mobile WiMax, cum ar fi: timp de stabilizare redus, supracreştere minimă şi bandă de frecvențe specifică sistemelor mobile WiMax. Proiectarea filtrelor pe baza obiectivelor de optimizare contradictorii este realizată prin programare liniară şi prin programare semi-definită (SDP), împreună cu ajustarea corespunzătoare a unei serii de parametri de proiectare. Filtrele digitale cu răspuns finit la impuls (FIR), proiectate utilizând programarea liniară şi SDP, evidențiază rezultate mai bune decât alte metode comparabile de proiectare. Proiectarea bazată pe SDP oferă performanțe mai bune decât cea bazată pe programarea liniară.