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DESCRIBING FUNCTION ANALYSIS OF AN *LC* OSCILLATOR STRUCTURE

BY

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Abstract. A detailed analysis based on the describing function approach of an *LC* oscillator having the same functionality as the classic CMOS Colpitts oscillator is presented. The advantages of this *LC* oscillator in comparison with the classic CMOS Colpitts oscillator are illustrated with simulation results. The Fourier integrals to determine the dc and fundamental components of the transistor current passing through the oscillator's tank are calculated. The theoretical results are in good agreement with the computer simulation..

Key words: *LC* oscillator; oscillator voltage amplitude; oscillator analysis; nonlinear equations; conduction angle; current–voltage MOS characteristics; describing function; Fourier integrals.

1. Introduction

The CMOS Colpitts oscillator shown in Fig.1 is an important block in RF circuits (Hajimiri & Lee, 1998, 1999; Andreani *et al.*, 2005). The oscillation frequency and the minimum required gain for the oscillations to build up are calculated by Jones & Martin (2007).

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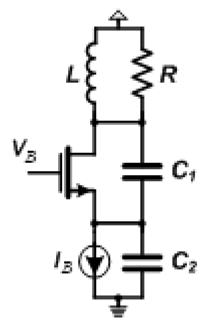

Fig. 1 – CMOS Colpitts oscillator.

One drawback of the CMOS Colpitts oscillator is that the amplitude of the oscillation depends on the current passing through the MOS transistor. The value of this current is limited by the current–voltage MOS transistor characteristic.

Another drawback of the simple CMOS Colpitts oscillator is given by the fact that the $C_1 - C_2$ capacitive divider is loaded by the equivalent impedance seen at the source of transistor. Its expression is

$$\frac{1}{g_m + \dfrac{s^3[(C_1+C_2)C_1RL - LC_1^2] + s^2[(C_1+C_2)L - LC_1g_m] + s(C_1+C_2)R}{s^2LC_1R + sL + R}}. \quad (1)$$

As a result, the voltage at the transistor's source is not exactly in phase with the voltage at its drain. For the two voltages to be in phase so to have a positive feedback it is necessary that this equivalent impedance to be much larger than the reactance of C_2 capacitance. Because the equivalent resistance seen at the source of M transistor is usually small, a large C_2 value is required, which implies a large area consumption.

Another drawback of the circuit in Fig.1 is that its frequency of oscillation is a function of the transistor's transconductance

$$\omega_0^2 = \frac{g_mL + R(C_1+C_2)}{RC_1C_2L}. \quad (2)$$

Because of g_m dependence with temperature the frequency of oscillation varies accordingly.

Fig. 2 shows a modified CMOS Colpitts oscillator in which the above three mentioned problems are solved.

The principle of operation is similar to the one in the case of classic CMOS Colpitts oscillator. The proposed structure is realized with two transistors in the signal path, M_1 and M_2.

The voltage sources, V_B , are needed in order to bias M_1 – M_2 into saturation. In order that these sources not to shunt at ground C_2 capacitor at large frequencies of operation, a large resistor R_B of value 100 kΩ is inserted in series with them.

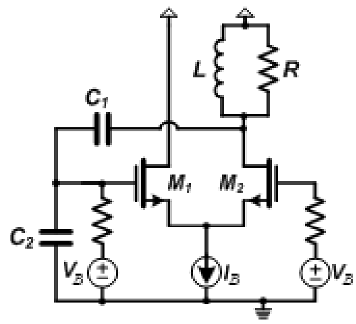

Fig.2 – Modified CMOS Colpitts oscillator.

The signal at the drain of M_2 transistor is coupled *via* C_1 and C_2 capacitors to the gate of M_1 transistor thus the C_1 – C_2 capacitive divider is not loaded. The amplitude of the oscillation at the drain of M_2 transistor is limited because this transistor will cut off if all the bias current passes through M_1 transistor.

One advantage of the proposed structure consists on the fact that the current through M_2 transistor could not grow more than the value of the bias current source, I_B. In the case of simple CMOS Colpitts oscillator the value of the current passing through the oscillator's tank is limited by the MOS transistor's current–voltage characteristic. By choosing appropriate values for the I_B bias current source it is possible to keep the transistors of the proposed scheme out of the triode region which increases the frequency of operation.

By opening the feedback loop and inserting at the gate of M_1 transistor an input small-signal voltage source, we obtain the closed-loop gain

$$\frac{v_{\text{out}}}{v_{\text{in}}}=\frac{sLR(C_1+C_2)}{s^2[2LRC_1^2-2C_1LR(C_1+C_2)]+s[g_mC_1LR-2L(C_1+C_2)]-2(C_1+C_2)R}, \tag{3}$$

where $g_{m1} = g_{m2} = g_m$ represents the transconductances of M_1 and M_2 transistors for identical bias conditions and v_{out} is taken from the drain of M_2 transistor. From relation (3) it results that the circuit oscillates if the closed-loop transfer function goes to infinity at an imaginary value of s, (s = jω_0). As a result both real and imaginary parts of the denominator must drop to zero at this frequency. By equalizing the imaginary part of the denominator with zero, it results the minimum required gain for the near-sinusoidal oscillations to build up

$$g_mR=2\left(1+\frac{C_2}{C_1}\right). \tag{4}$$

For equal values of C_1 and C_2, the minimum required gain is equal to 4 which is identical to the result obtained in the case of classic CMOS Colpitts oscillator (Jones & Martin, 2007).

Next, the frequency of oscillation is determined by equalizing the real part of the denominator with zero

$$\omega_0^2 = \frac{1}{L C_1 C_2 / (C_1 + C_2)}. \tag{5}$$

From (5) it is seen that the frequency of operation of the proposed structure is no longer a function of the transistor's transconductance. As a result, lower values for capacitances can be chosen to obtain the same frequency of oscillation as in the case of the classic CMOS Colpitts oscillator.

For equal values of circuit parameters and assuming the two capacitances are equal, $C_1 = C_2 = C$, it is calculated the n value which represents how much the capacitances could be scaled down in the case of the proposed oscillator to obtain the same frequency of oscillation as in the case of classic CMOS Colpitts oscillator

$$n = 1 + \frac{g_m L}{2RC}. \tag{6}$$

From relation (6) it is seen that n is larger than unity which proves the fact that in order for the two types of oscillators to have the same frequency of oscillation, lower values for the capacitances can be used for the proposed structure. For usual values of the device parameters, n lies in the interval [1.2; 2].

2. Detailed Analysis of the CMOS Colpitts Oscillator Circuit

The effect of the nonlinearity on the oscillation amplitude can be evaluated using the describing function approach (Gray *et al*., 2000). With the view to perform this analysis, a square-law MOS model (Razavi, 1992) is used to describe the current–voltage characteristics namely

$$I_d = \begin{cases} \dfrac{k'}{2} \cdot \dfrac{W}{L} (V_{gs} - V_T)^2, \ V_{gs} \geq V_T, \ V_{ds} \geq V_{gs} - V_T, \\ 0, \ V_{gs} < V_T, \end{cases} \tag{7}$$

where W is the channel width, L – the channel length and $k' = \mu_n C_{0x}$ – the gain parameter of the nMOS transistor. The threshold voltage, V_T, is considered to be a constant. From (7) the transistors are assumed to operate only in saturation and cut-off regions. The transistor's output resistances are neglected.

The oscillator's tank is assumed to have a high Q quality factor so only the fundamental component of the output voltage is of interest. This component is coupled *via* capacitors C_1 and C_2 to the gate of M_1 transistor.

By writing Kirchhoff second law across the loop formed by the gate sources of transistors M_1 and M_2 the following relation is obtained:

$$V_i - V_{gs1} + V_{gs2} - V_B = 0, \tag{8}$$

where V_i is the total voltage applied at the gate of M_1 transistor, *i.e.* $V_i = v_i + V_B$, and v_i is equal to a fraction of the output voltage fundamental

$$v_i = \frac{C_1}{C_1 + C_2} V_{\text{out}} \cos\omega_0 t = V_A \cos\omega_0 t \text{, where } V_A = \frac{C_1}{C_1 + C_2} V_{\text{out}} .$$

Having in view the results obtained by Razavi (1992), after some rearrangements the drain current of M_2 transistor results as being equal to

$$I_{d2} = \begin{cases} I_B, \; v_i \le -v_{\max}, \\ \dfrac{I_B}{2} - \dfrac{v_i}{2}\left[k^{'}\dfrac{W}{L}\left(I_B - v_i^2 \dfrac{k^{'}W}{4L}\right)\right]^{1/2}, -v_{\max} \le v_i \le v_{\max}, \\ 0, \; v_i \ge v_{\max}, \end{cases} \tag{9}$$

where $v_{\max} = \left(\dfrac{2I_B}{k^{'}W/L}\right)^{1/2}$.

The normalized drain current with respect to the bias current source, I_B, is

$$\frac{I_{d2}}{I_B} = \begin{cases} 1, \; v_{\text{in}} \le -1, \\ \dfrac{1}{2} - \dfrac{v_{\text{in}}}{\sqrt{2}}\left(1 - \dfrac{v_{\text{in}}^2}{2}\right)^{1/2}, \; -1 \le v_{\text{in}} \le 1, \\ 0, \; v_{\text{in}} \ge 1, \end{cases} \tag{10}$$

where $v_{\text{in}} = v_i / v_{\max}$.

Next the dc and fundamental components of the drain current are obtained. To simplify the analysis we utilize the notations: $\theta = \omega_{0t}$, $a = V_A/v_{\max}$. With these notations the drain current can be written

$$I_{d2} = \begin{cases} 1, \; a\cos\theta \le -1, \\ \dfrac{1}{2} - \dfrac{a\cos\theta}{2}\left[1 - \dfrac{(a\cos\theta)^2}{2}\right]^{1/2}, \; -1 \le a\cos\theta \le 1, \\ 0, \; a\cos\theta \ge 1. \end{cases} \tag{11}$$

The condition $a\cos\theta \ge 1$ can be described by a cut-off angle defined as $\cos\theta_{\text{off}} = 1/a$. Similarly, the condition $a\cos\theta \le -1$ can be described by a conduction angle defined as $\cos\theta_{\text{on}} = -1/a$. The drain current through M_2 transistor normalized to the bias current source I_B value now becomes

$$\frac{I_{d2}}{I_B} = \begin{cases} 0, \; 0 \le \theta \le \theta_{\text{off}}, \\ \dfrac{1}{2} - \dfrac{a\cos\theta}{2}\left[1 - \dfrac{(a\cos\theta)^2}{2}\right]^{1/2}, \; \theta_{\text{off}} \le \theta \le \theta_{\text{on}}, \\ 1, \; \theta_{\text{on}} \le \theta \le 2\pi - \theta_{\text{on}}, \\ \dfrac{1}{2} - \dfrac{a\cos\theta}{2}\left[1 - \dfrac{(a\cos\theta)^2}{2}\right]^{1/2}, \; 2\pi - \theta_{\text{on}} \le \theta \le 2\pi - \theta_{\text{off}}, \\ 0, \; 2\pi - \theta_{\text{off}} \le \theta \le 2\pi. \end{cases} \tag{12}$$

The dc Fourier coefficient normalized to the bias current source I_B value is given by relation

$$I_{d2,\text{dc}} = \frac{1}{2\pi}\int_0^{2\pi} \frac{I_{d2}}{I_B}\,\mathrm{d}\theta. \tag{13}$$

The fundamental component of the current normalized to the bias current source I_B value for $\theta_{\text{off}} = \arccos(1/a)$ and $\theta_{\text{on}} = \pi - \arccos(1/a)$ is

$$I_{d2,1} = \frac{1}{\pi}\int_0^{2\pi} \frac{I_{d2}}{I_B}\cos\theta\,\mathrm{d}\theta\,. \tag{14}$$

Next, the fundamental component of the M_2 transistor's drain voltage at the resonance frequency as a function of the fundamental component of the M_2 transistor's current is calculated. The equivalent impedance seen from the drain of M_2 transistor is

$$Z_{\text{in}} = sL \,||\, R \,||\, \frac{1}{sC_{\text{eq}}}, \tag{15}$$

where $C_{eq} = C_1C_2/(C_1 + C_2)$. It result that

$$Z_{in} = \frac{sLR}{s^2LRC_{eq} + sL + R}\,. \quad (16)$$

For the frequency of oscillation, the impedance seen at the output node becomes

$$Z_{in|s=j\omega_0} = \frac{j\omega_0 LR}{j\omega_0 L + (r - \omega_0^2 LRC_{eq})}\,. \quad (17)$$

For equal values for the two capacitances and for $\omega_0 = \sqrt{2/LC}$

$$Z_{in|s=j\omega_0, C_1=C_2} = R\,. \quad (17)$$

From (18) the fundamental component of the oscillation voltage at the frequency of oscillation becomes

$$V_{out} = RI_{d2}. \quad (19)$$

Relation (19) gives the magnitude of the fundamental of the oscillation voltage over the magnitude of the fundamental of the M_2 transistor current.

3. Simulation Results

In order to illustrate the advantages of the proposed structure regarding the limitation of the amplitude of the current passing through the oscillator's tank, the proposed *LC* oscillator was simulated in a TSMC 3V3 180 nm technology.

The simulation results, along with the circuit and device parameters in the case of proposed *LC* oscillator, are given in Table1.

Table 1

L uH	C_1 pF	C_2 pF	I_B uA	W/L	VDD V	g_{mM2} mS	k' uA/V	T_{osc} ns	f_{osc} MHz
100	50	100	100	2u/720	3.3	1.274	120	377	2.7

The M_2 drain current waveform as well as the drain output voltage waveform *versus* time are shown in Figs.3 and 4, respectively.

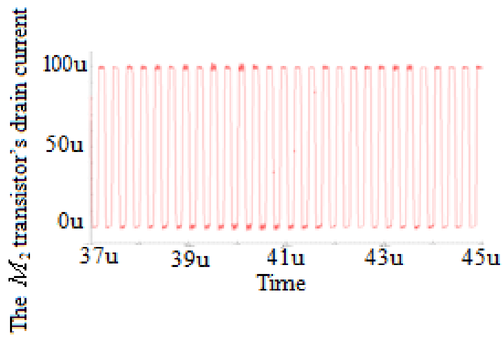

Fig. 3 – The M_2 transistor's drain current waveform *versus* time.

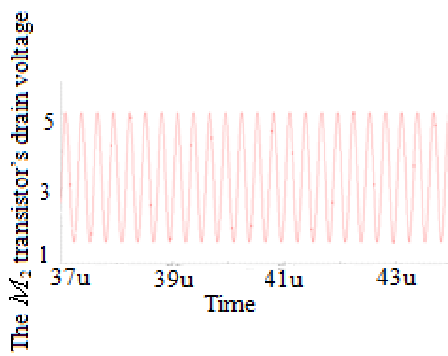

Fig. 4 – The M_2 transistor's drain voltage waveform *versus* time.

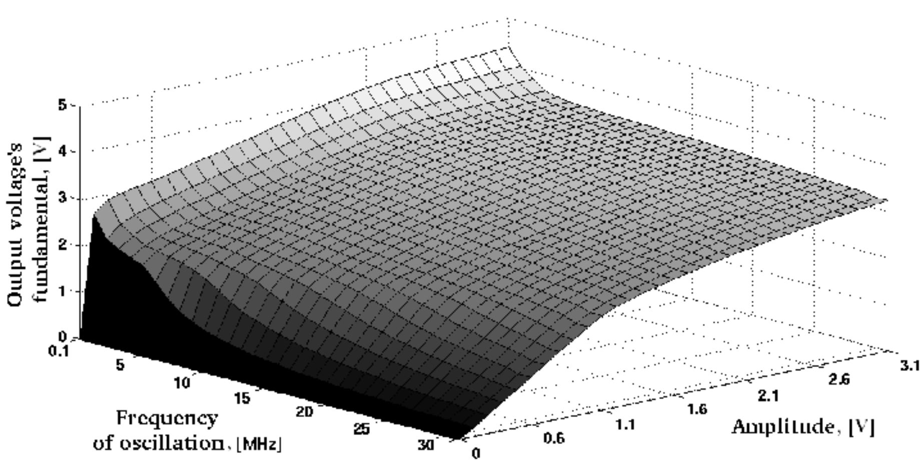

Fig. 5 – The output voltage's fundamental as a function of amplitude and frequency of the voltage at the M_1 transistor's gate.

From the simulations it is seen that the amplitude of the M_2 transistor's current ranges between 0 A and 200 uA which is the value of the bias current source, I_B.

A third plot in MATLAB of the fundamental of the output voltage at the drain of M_2 transistor as a function of the amplitude and frequency of the voltage at the gate of M_1 transistor is shown in Fig.5.

4. Conclusions

1. A new *LC* oscillator was proposed. The minimum required gain for the oscillations to build up and the frequency of oscillation are calculated and compared to those in the case of classic CMOS Colpitts oscillator.

2. One advantage of the proposed structure in comparison with the simple CMOS Colpitts oscillator is that the current passing through the oscillator's tank could not grow more than the value of the bias current source. In the case of the simple CMOS Colpitts oscillator the current passing through oscillator's tank is limited by the MOS transistor voltage–current characteristic.

3. Another advantage of the proposed scheme is that smaller values for the capacitances are needed in order to obtain the same frequency of oscillation as in the case of classic CMOS Colpitts oscillator.

4. The quality factors of the two circuits are calculated. The quality factor of the modified CMOS Colpitts oscillator is higher than the one factor of the classic CMOS Colpitts oscillator.

5. The expressions for the dc and the fundamental components of the current passing through the *LR* tank are determined. To simplify the analyses the transistor is assumed to be in only two regions of operation: saturation and cut-off. The fundamental component of the output voltage as a function of the fundamental component of the M_2 drain current is calculated.

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ANALIZĂ BAZATĂ PE METODA FUNCŢIEI DE DESCRIERE A UNEI STRUCTURI DE OSCILATOR *LC*

(Rezumat)

A fost propusă o nouă structură de oscilator de tip *LC* având o funcţionare similară cu cea din cazul oscilatorului Colpitts. Schema propusă prezintă unele avantaje faţă de oscilatorul Colpitts şi anume:

1. Frecvenţa de oscilaţie nu depinde de transconductanţa tranzistoarelor.
2. Se pot alege valori mai mici pentru capacităţi pentru a obţine, în condiţii de polarizare identice, aceeaşi frecvenţă de oscilaţie ca în cazul oscilatorului Colpitts.
3. Factorul de calitate al oscilatorului propus este mai mare decât cel al oscilatorului Colpitts.
4. Curentul prin tranzistoarele M_1–M_2 este limitat de valoarea sursei de polarizare, I_B.

În ciuda faptului că circuitul propus poate fi simulat cu uşurinţă, o metodă de calcul a amplitudinii de oscilaţie bazată pe conceptul de funcţie de descriere, este necesară pentru a avea un punct de pornire în proiectarea unui astfel de circuit sau pentru a avea un model comportamental într-o metodologie de proiectare de tip *top-down*. Metoda de analiză cuprinde patru paşi:

1. Constrângerile circuitului.
2. Caracteristica tranzistorului în toate regiunile de funcţionare.
3. Legătura dintre regiunea de funcţionare a tranzistorului de faza tensiunii de ieşire a oscilatorului.
4. Calculul integralelor Fourier pentru a determina componentele de curent continuu şi fundamentala curentului prin tranzistor.

S-a determinat, urmărind paşii anterior menţionaţi, relaţia dintre fundamentala tensiunii din nodul de ieşire în funcţie de fundamentala curentului de drenă al tranzistorului M_2.