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ON DISTORTIONS IN A TUNABLE CMOS TRANSCONDUCTOR

BY

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Abstract. In this paper, we discuss characteristics and simulation results for a tunable fully differential CMOS transconductor (OTA) designed in an AMS 0.18 μm CMOS technology following an architecture recently proposed by Tien-Yu Lo *et al*. The investigations envisaged the OTA behavior with respect to the amplitude and frequency of the input signal as well as to the load. THD and IP3 dependence on frequency are presented.

Key words: CMOS; transconductor; nonlinearity; frequency response.

1. Introduction

The use of fixed or tunable OTA’s in integrated circuits design has no need to be emphasized; they have various applications as building blocks for filters (Tien-Yu Lo *et al*., 2009; Geiger & Sánchez-Sinencio, 1985), oscillators (Razavi, 2001), analog master-slave circuits, etc. A recent OTA application in a channel selection filter for multi-mode direct-conversion radio receivers has been presented in (Tien-Yu Lo *et al*., 2009) with an implementation in TSMC 0.18 μm technology.

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The core building block in the above mentioned work is a large range tunable fully differential OTA based on a translinear loop. The authors show that the use of differential OTA's significantly improve performances compared to conventional MOSFET-resistor or MOSFET only transconductors. The aim of this paper is to report an independent design of the architecture proposed in (Tien-Yu Lo *et al*., 2009) for the tunable transconductor optimized with respect to linearity and to study its frequency behavior for large signal operation. Moreover, comparison with IP3 results is also made.

2. Circuit Principle

The core schematic of the tunable differential OTA is presented in Fig. 1.

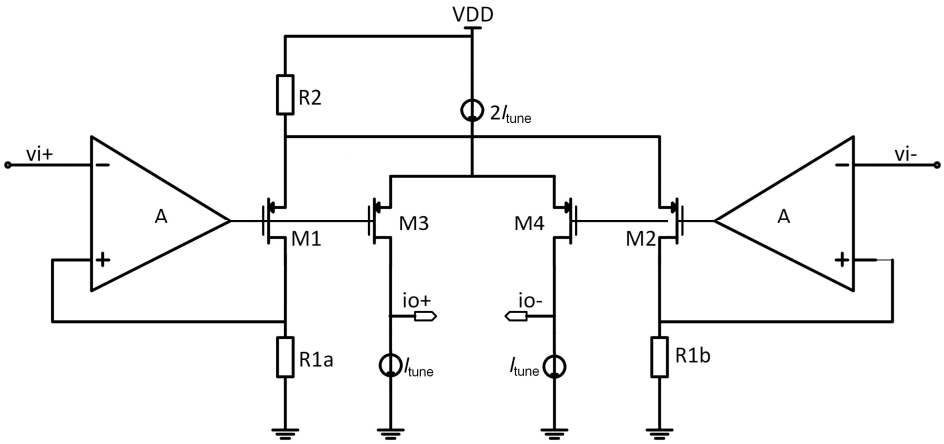

Fig. 1 – Principle of OTA schematic (adapted from Tien-Yu Lo *et al*., (2009)).

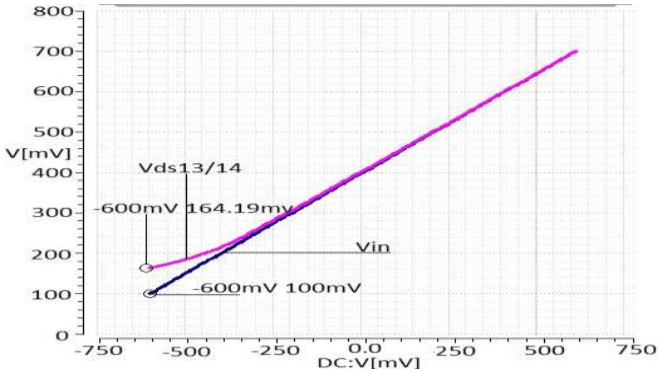

Fig. 2 – Ideal and triode transistor based conversion (M13 and M14 in Fig. 3) of input voltage to resistor voltage (the maximum error is 64.19 mV).

The above circuit performs two tasks, one to convert the input voltage to current and the other one to make a current multiplication by means of a

translinear loop (Lopez-Martin & Carlosena**,** 2001). Roughly, the precision of the voltage to current conversion is thus determined first by the (non)linearity of the voltage to current dependency of the triode biased transistors that will finally replace the resistors R1a and R1b (see Fig. 2) and second by the current multiplication errors. Since we do not envisage a rail to rail functionality this offset does not matter significantly. Transistors M1 and M2 work in all cases in weak inversion while M3 and M4 work for small Gm (small current I_{tune}) in weak inversion and for high Gm (high current I_{tune}) in strong inversion, where Gm represent the transconductance of the OTA. It follows, from Fig. 2, that the voltage to current conversion will not be perfect when using triode biased transistors.

Both circumstances are discussed by Tien-Yu Lo *et al.*, (2009) where it is shown that in the first case the transconductance is proportional to I_{tune} while in the second one, proportional to the square root of I_{tune}.

3. Circuit Architecture

The schematic of the differential OTA is represented in Fig. 3. The circuit has been independently designed following the same architecture as by Tien-Yu Lo *et al.*, (2009), but in an AMS 0.18 µ CMOS technology and all simulations have been done using transistor level current sources as shown in Fig. 3.

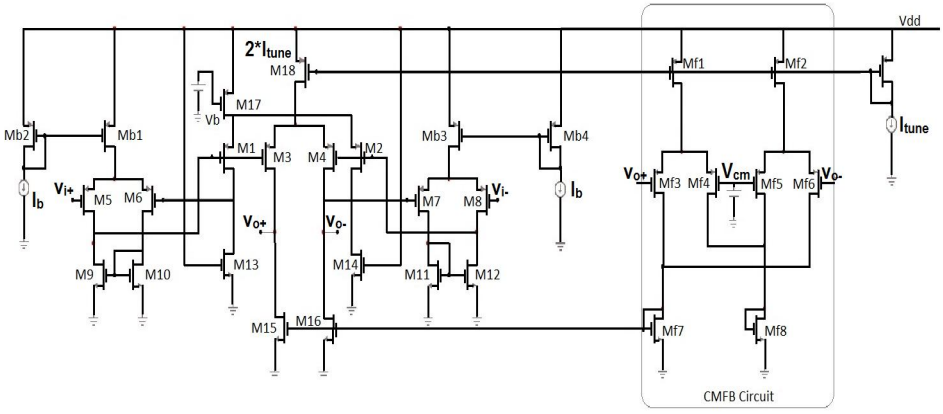

Fig. 3 – Schematic of the OTA implementation based on Tien-Yu Lo *et al.*, (2009).

4. Large Signal Distortion Analysis

The main features of the designed OTA are summarized in Table 1.

The DC characteristics for an input voltage in the range –0.6 V to +0.6V, I_{tune} from 1 µA to 100 µA and common mode voltage of 0.4 V are presented in Fig. 4 where the output current has been plotted. The variation of Gm with the tuning current is shown in Fig. 5.

Table 1
Performances of Designed OTA

Parameter	Value
Technology	AMS 0.18μm
Power supply	1.2V
Tuning ratio [Gm_{max}/Gm_{min}]	35
Gm	[3.12-109.98μS]
HD3	–52dB
THD @[1Hz…100MHz, Av = 500mVpp]	< 1%
Power Consumption	0.072 mW @[I_{tune}=1uA] 0.44 mW @[I_{tune}=100uA]

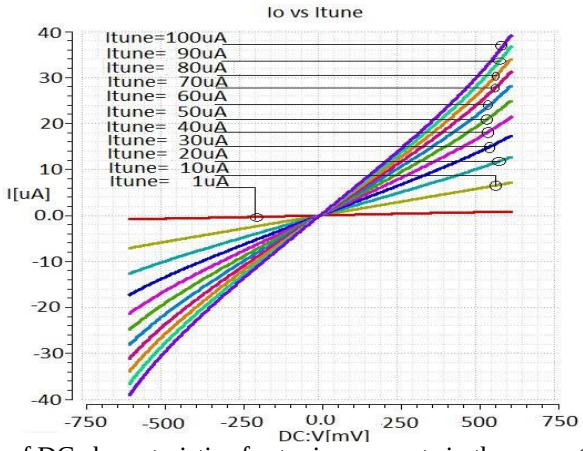

Fig. 4 – Family of DC characteristics for tuning currents in the range 1 μA,…,100 μA.

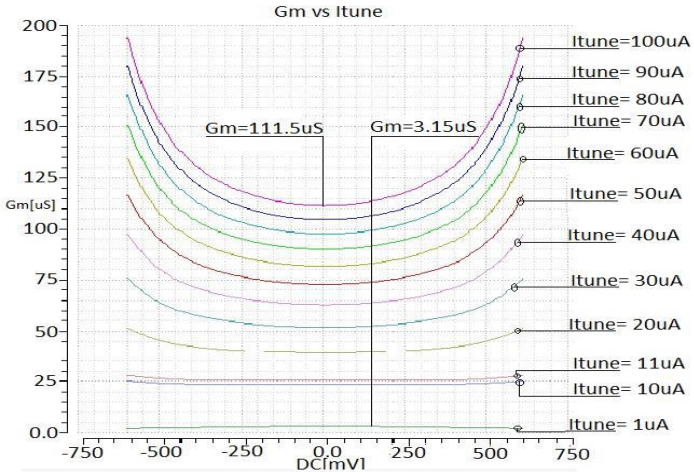

Fig. 5 – Variation of Gm with bias and I_{tune}.

A particular aspect investigated in this paper refers to large signal distortion analysis. It well known that distortion is an important aspect related to OTA design (Ismail & Fiez, 1994; Colombo *et al*., 2011; Wambacq & Sansen, 1998; Ha Le-Thai *et al*., 2010). In what follows we give more results regarding distortion by plotting the THD dependence both on amplitude and frequency (Figs. 6,…,9) for two values of the resistive load and for two extreme values of the tuning currents. Further on we will show several results obtained with IP3.

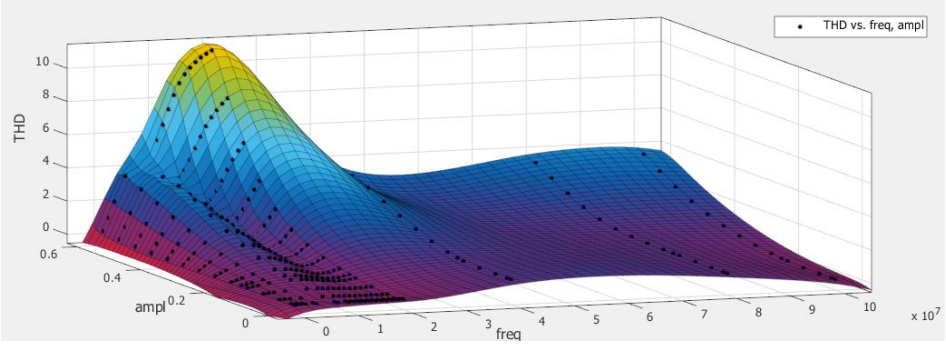

Fig. 6 – THD *vs.* frequency and amplitude (I_{tune} = 1 μA, Rl = 50 Ω).

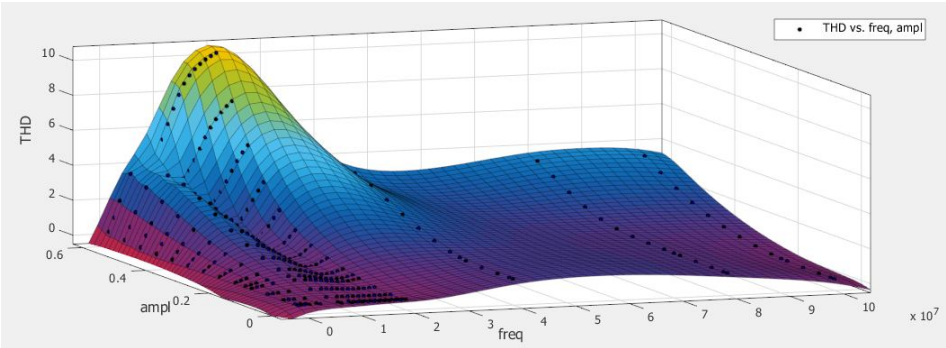

Fig. 7 – THD *vs.* frequency and amplitude (I_{tune} = 1 μA, Rl =1 KΩ).

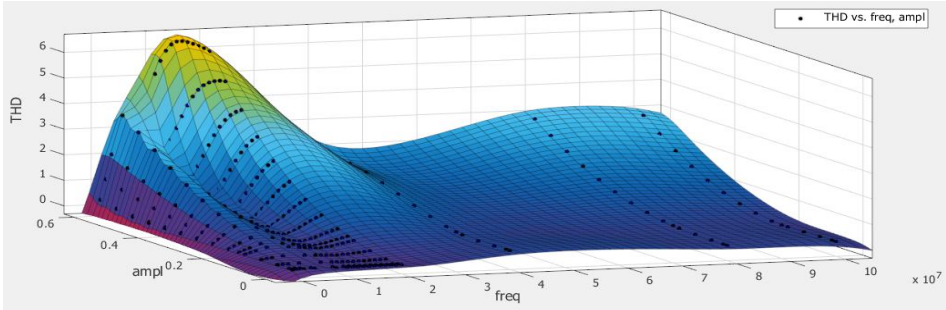

Fig. 8 – THD *vs.* frequency and amplitude (I_{tune} = 100 μA, Rl = 1 KΩ).

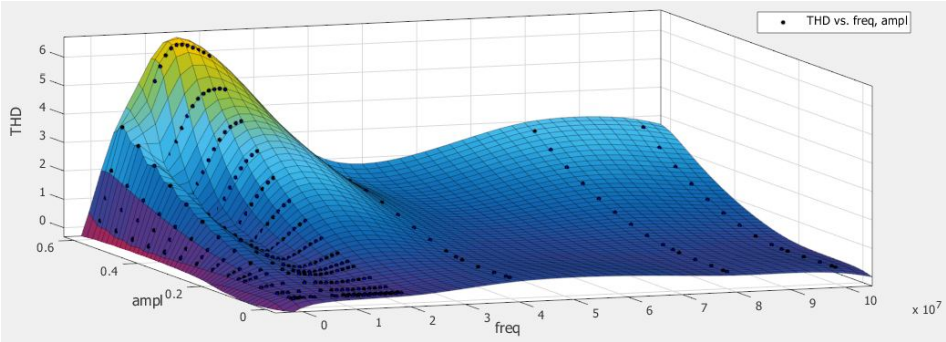

Fig. 9 – THD *vs.* frequency and amplitude (I_{tune} = 100 μA, Rl = 50 Ω).

We consider that this kind of distortion characterization gives more insight regarding the nonideal behavior of an OTA. The interesting and intriguing aspect of the THD plots is their shape around the frequency of about 20 MHz. Even though it is well known that the AC analysis gives no information related to distortion we have run an AC and a PZ simulation and found a peak in the frequency response due to the pair of complex conjugate poles $p_{1,2}$ = 3.88511e7±5.18053e7 with a quality factor Q = 0.833.

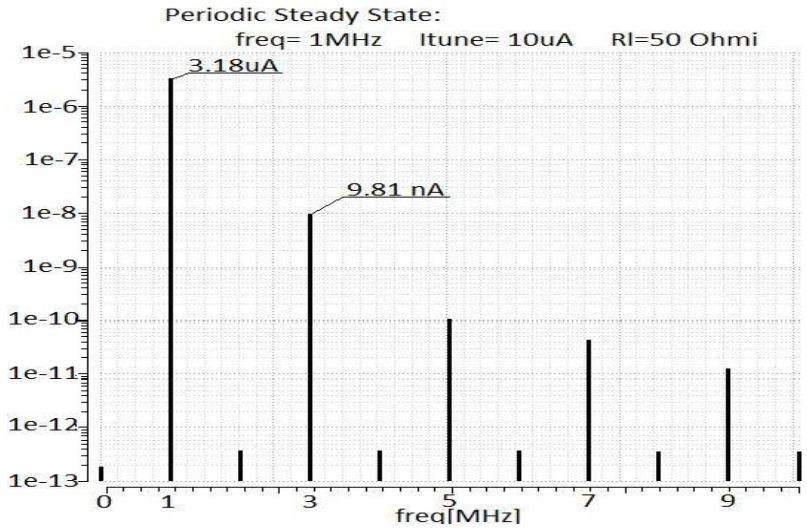

Fig. 10 – Output spectrum for I_{tune} =10 μA.

This result leads to the conclusion that the observed shape of the THD can be (partially) explained by the fact that for certain frequencies the third harmonic is “amplified”. This hypothesis has been confirmed by two Periodic Steady State (PSS) simulations (Figs. 10 and 11) with the same input level, one for a frequency of 1 MHz and the other one for 20 MHz when the third harmonic is in the range of the AC peak determined by the complex poles. It is

apparent that in the second case the third harmonic is more than three times higher explaining the higher THD around the frequency of 20 MHz. Globally, it is apparent that for amplitudes less than 0.5 Vpp and frequencies up to 100 MHz the THD does not exceed 1%.

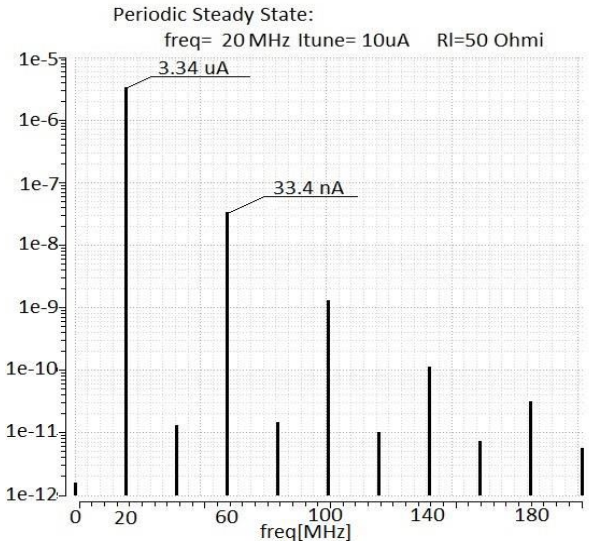

Fig. 11 Output spectrum for I_{tune}=10 μA

In the following we analyze the nonlinearity of the circuit using the well known classical IP3 analysis (Ha Le-Thai *et al*., 2010; Mobarak, 2010; Chamla *et al*., 2005; Keng Leong Fong, 2000; Terrovitis & Meyer, 2000) for two frequencies: 1 MHz and 20 MHz chosen in a low respectively high THD region. The IP3 analysis used for bandpass circuits implies injecting two close input frequencies as shown in Fig. 12 and calculating the amplitude of the fundamental tones for which the intermodulation components have the same magnitude. The main difference between the two methods is that THD refers to wide band amplifiers while IP3 to narrow band ones. However, simulations show that the THD results qualitatively correspond to those obtained using IP3.

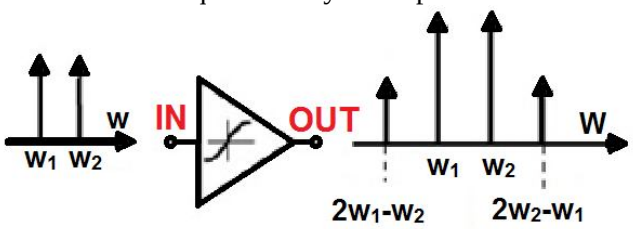

Fig. 12 –Behavior of a nonlinear system for two input signals.

The two simulations have been done using the frequencies (1 MHz, 1.1 MHz) and (20 MHz, 20.1 MHz), respectively. The results presented in

Fig. 13 shows that the amplitudes corresponding to the IP3 intersections satisfy the relationship $A_{IIP3,20MHz} = 0.55\ A_{IIP3,1MHz}$ which confirms qualitatively the THD results (higher distortion for 20 MHz corresponds to lower A_{IIP3}).

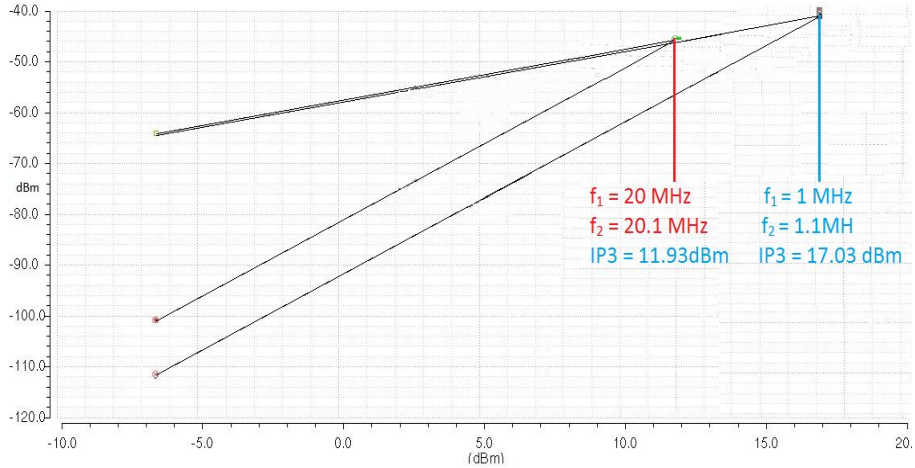

Fig. 13 – IP3 simulation for 1 and 20 MHz inputs tones and $I_{tune} = 10$ µA.

5. Concluding Remarks

A fully differential tunable OTA has been designed in an AMS 0.18µm CMOS technology and investigated from the point of view of large signal distortion using plots of the THD *vs*. amplitude and frequency as well as the IP3. Besides, the remarkable OTA characteristics, the THD plot *vs*. both amplitude and frequency proves to be a significant tool for describing the nonidealities of the circuit, the results qualitatively fitting those given by IP3.

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STUDIUL DISTORSIUNILOR UNUI TRANSCONDUCTOR CMOS CONTROLABIL

(Rezumat)

Se analizează caracteristicile şi rezultatele de simulare pentru un transconductor CMOS complet diferenţial (OTA) proiectat în tehnologie AMS CMOS 0,18 μm, bazată pe o arhitectură propusă recent de Tien-Yu Lo. Cercetarea a vizat studiul comportamentului transconductorului raportat la amplitudinea şi frecvenţa semnalului de intrare precum şi sarcină. THD şi IP3 sunt este de asemenea studiaţi.