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A CMOS CURRENT REFERENCE CIRCUIT WITHOUT RESISTORS

BY

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Abstract. A method of obtaining reference currents in CMOS circuits without resistors is presented. The proposed circuit is implemented in 65 nm CMOS standard technology and operates with voltage supply in the range [2.2… 2.8] V from –25°C to +130°C. The reference current is 1 µA ± 1 nA, has a temperature coefficient of 12.9 ppm/ºC and a line sensitivity of 8.7 nA/V. The circuit has also a good power supply rejection rate (–164 dB at low frequencies).

Key words: current reference; temperature coefficient; line sensitivity; power supply rejection rate.

1. Introduction

Most of CMOS current reference circuits are based on summing currents with negative and positive temperature coefficients.

The emitter-base voltage V_{EB} of bipolar transistors and the difference between two V_{EB} (the thermal voltage V_T) have thermal characteristics that are usually exploited in generating currents with negative and positive temperature gradients; V_{EB} decreases approximately linear with temperature (–2 mV/ºC) while V_T increases linearly with temperature (+0.085 mV/ºC).

The conversion of voltages like V_{EB} and V_T into currents can be carried

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out *via* resistors (Imbrea *et al*., 2013), *via* MOS transistors operating in triode regime (De Vita *et al.*, 2007) or via active MOS transistors (Imbrea *et al*., 2013), (Falconi *et al*., 2007), (Quemada *et al*., 2012).

The difference between currents with negative temperature coefficients may also produce reference currents (Zhao *et al*., 2012). Currents having negative temperature gradient are generated in (Liu *et al*., 2010) by means of the threshold difference between a thin and a thick oxide MOS transistor.

2. The Proposed Method to Generate a Reference Current and Circuit Description

The schematic of the circuit contains four parts as shown in Fig.1, namely start-up, I_{ptc} generator, I_{ntc} generator and output stage (I_{ptc} and I_{ntc} denote currents having positive and negative temperature coefficient, respectively). The start-up is necessary because I_{ptc} generator is self-biased. The nominal supply voltage is 2.5 V. The devices Q_1, Q_2, Q_3 and Q_4 are vertical PNP bipolar transistors. The channels of all MOS transistors are long enough so the length modulation can be ignored.

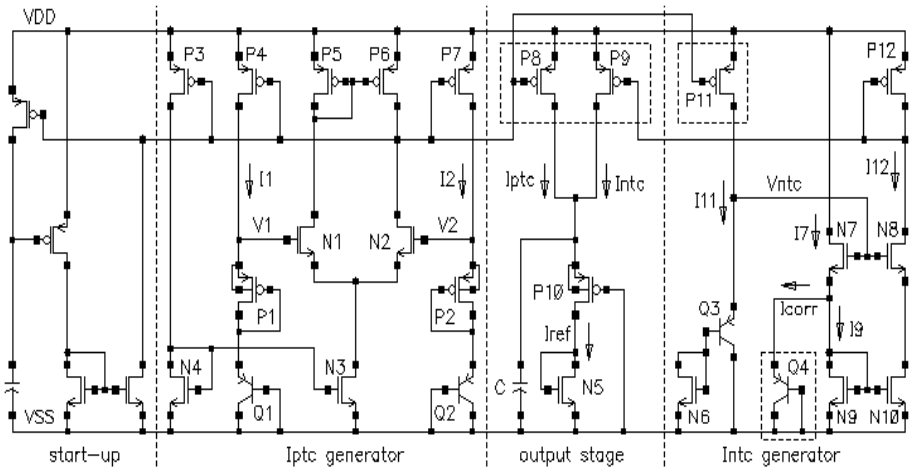

Fig. 1 – Schematic of the proposed current reference circuit.

The characteristic *I–V* of a MOS transistor working in the saturation region and strong inversion can be expressed as below

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2 = \frac{1}{2}K(V_{GS}-V_{TH})^2,\ K = \mu C_{ox}\frac{W}{L}, \qquad (1)$$

where μ is the mobility of charge carriers in the channel, C_{ox} – the oxide capacitance per unit area, W and L – the channel sizes and V_{TH} is the threshold voltage.

The I_{ptc} generator is similar with that presented in (Imbrea *et al*., 2013) and consists of a self-biased differential amplifier. No frequency compensation is needed for stability because the phase margin is greater than 60 degrees.

Starting from $V_1 = V_2$ and $I_1 = I_2$, constraints imposed by the amplifier, we obtain the following equations. Both transistors P_1 and P_2 are working in strong inversion

$$V_{SG(\mathrm{P}_1)} + V_{EB1} = V_{SG(\mathrm{P}_2)} + V_{EB2}, \tag{2}$$

$$V_{TH(\mathrm{P}_1)} + \sqrt{\frac{2I_1}{K_{\mathrm{P}_1}}} - V_{TH(\mathrm{P}_2)} - \sqrt{\frac{2I_2}{K_{\mathrm{P}_2}}} = V_T \ln N, \tag{3}$$

where: N represents the ratio between areas of Q_1 and Q_2. Assuming that $V_{TH(\mathrm{P}_1)}$ and $V_{TH(\mathrm{P}_2)}$ are equal, we obtain

$$\sqrt{I} = \frac{\sqrt{K_{\mathrm{P}_1}}\sqrt{K_{\mathrm{P}_2}}}{\sqrt{2}\left(\sqrt{K_{\mathrm{P}_2}} - \sqrt{K_{\mathrm{P}_1}}\right)} V_T \ln N, \tag{4}$$

where the letter I denote the common value of I_1 and I_2. Obviously, K_{P_2} must be greater than K_{P_1}. Eq. (4) may be expressed as

$$I = K_P V_T^2, \quad \sqrt{K_P} = \frac{\sqrt{K_{\mathrm{P}_1}}\sqrt{K_{\mathrm{P}_2}} \ln N}{\sqrt{2}\left(\sqrt{K_{\mathrm{P}_2}} - \sqrt{K_{\mathrm{P}_1}}\right)}. \tag{5}$$

The term $K_P V_T$ in eq. (5) is nearly constant with temperature so the current I has a positive temperature coefficient, being approximately proportional to the absolute temperature T. The current I_{ptc} injected in the output stage, proportional to I, is obtained by choosing a proper width W for the transistor P_8.

The I_{ntc} generator uses as input a voltage V_{ntc} with negative temperature coefficient; it is produced by P_{11}, Q_3 and N_6. The current I_{11} has to be properly adjusted by means of P_{11} width. The basic equations that describe the I_{ntc} generator are presented below.

$$\begin{cases} V_{ntc} = V_{GS(\mathrm{N}_7)} + V_{GS(\mathrm{N}_9)} = V_{TH(\mathrm{N}_7)} + \sqrt{\dfrac{2I_7}{K_{N_7}}} + V_{TH(\mathrm{N}_9)} + \sqrt{\dfrac{2I_9}{K_{\mathrm{N}_9}}}, \\ V_{EB4} = V_{GS(\mathrm{N}_9)}, \\ I_{\mathrm{Q}_4} = I_{\mathrm{corr}} \cong I_S \exp\dfrac{V_{GS(\mathrm{N}_9)}}{V_T}, \\ I_9 = I_7 - I_{\mathrm{corr}} = I_{12}. \end{cases} \tag{6}$$

where: I_{Q_4} is a correction current and, for this reason, it is also named I_{corr}. The term I_S denotes the saturation current of a bipolar junction.

It is well known that the threshold voltage of all MOS transistors decreases approximately linear with temperature. The input voltage V_{ntc} also forces $K_{GS(N_7)}$ and $K_{GS(N_9)}$ to decrease with temperature. From eq. (6) we derive the following equation

$$\frac{1}{2}K_{N_7}(V_{ntc}-V_{GS(N_9)}-V_{TH(N_7)})^2 - I_S \exp\frac{V_{GS(N_9)}}{V_T} = \frac{1}{2}K_{N_9}(V_{GS(N_9)}-V_{TH(N_9)})^2 = I_{12}. \quad (7)$$

Solving eq. (7) analitically, in order to get a linear decrease with temperature for the current I_{12}, is a very difficult task. However, we can find the proper sizes of the transistors P_{11}, N_7, N_9 and Q_4 by simulations (P_{11} helps produce the required input voltage V_{ntc}). Note that N_8 and N_{10} have the same sizes as N_7 and N_9, respectively. One solution for eq. (7), based on simulations, is shown in Fig. 2.

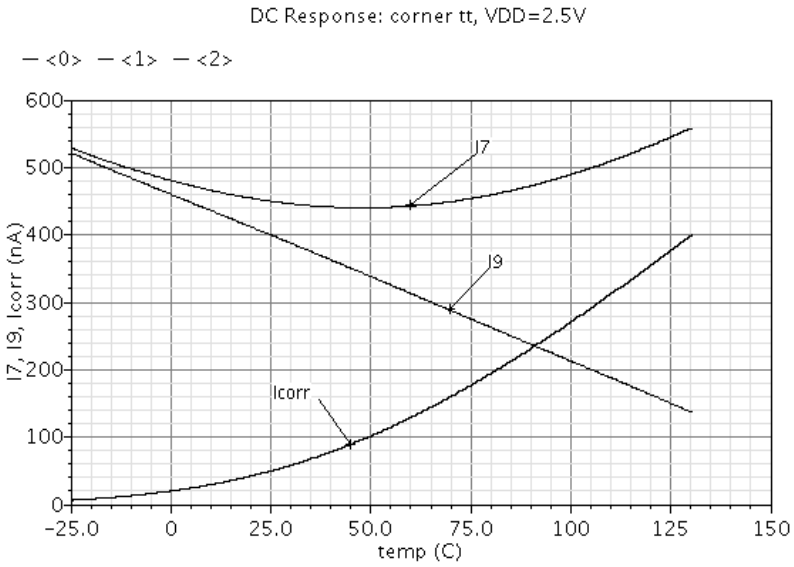

Fig. 2 – A desired solution for I_{ntc} generator.

The current I_{ntc} injected in the output stage is proportional to I_{12} and it is obtained by choosing a proper width W for the transistor P_9.
The output stage implements the equation

$$I_{ref} = I_{ptc} + I_{ntc}. \quad (8)$$

The capacitor C (about 4 pF) and the active transistor P_8 form together a filter that improves the power supply rejection rate at high frequencies.

3. Simulation Results

The DC response corresponding to typical corner and 2.5 V supply voltage is illustrated in Fig. 3. The circuit generates a reference current I_{ref} very close to 1 µA. The temperature coefficient (TC) of I_{ref} is 12.9 ppm/ºC in the range [–25…+130]ºC. Note that TC drops to half (6.5 ppm/ºC) in the temperature range [–18… +128]ºC.

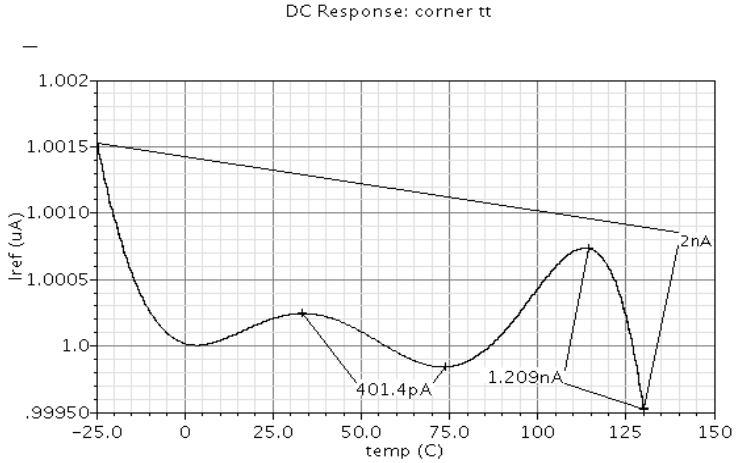

Fig. 3 – Influence of temperature on the reference current.

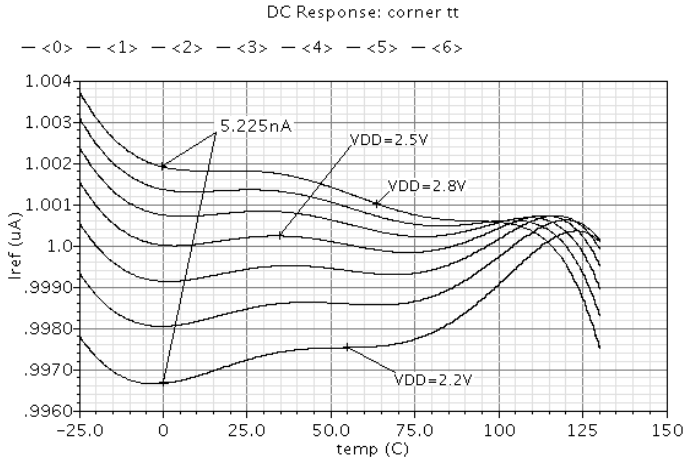

Fig. 4 – Line sensitivity.

The influence of the supply voltage V_{DD} on I_{ref} (also called *line sensitivity*) is shown in Fig. 4. If V_{DD} changes between 2.2 V and 2.8 V, which means 2.5 V ± 12%, then I_{ref} has maximum deviations of –3.2 nA and +2 nA from the nominal values. This means a line sensitivity of about 8.7 nA/V.

Technological process variations affect significantly the current I_{ref}. At low temperatures the values of I_{ref} vary much from the typical ones (–28% in slow-slow corner and +43% in fast-fast corner). Also, TC greatly increases. However, the process variations can be compensated by trimming the sizes of transistors marked in Fig. 1 with dashed rectangles, namely P_8, P_9, P_{11} and Q_4. The result is presented in Fig. 5. After adjusting the width of P_8, P_9, P_{11} and the multiplicity factor of Q_4 the two extreme corners, ss and ff, move very close to the typical one.

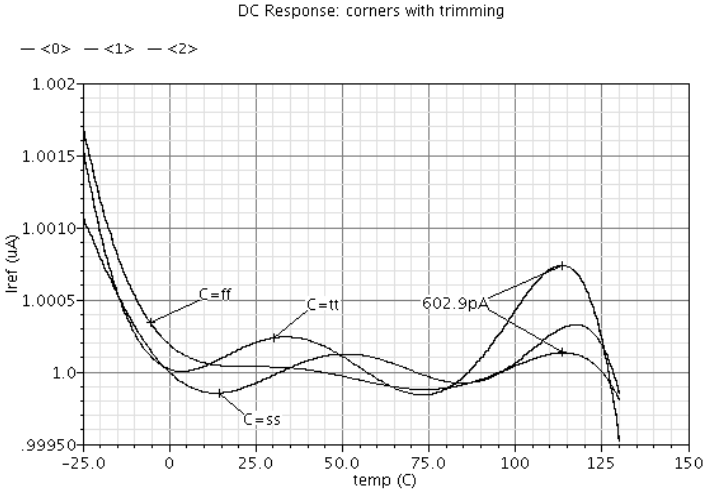

Fig. 5 – Compensation of process variations by trimming.

The mismatch between transistors also affects the current I_{ref}. Monte Carlo simulations are shown in Fig. 6. Some correlations between transistors were considered. The ratio *standard deviation/mean* (sd/mu) of I_{ref} is 3.23%.

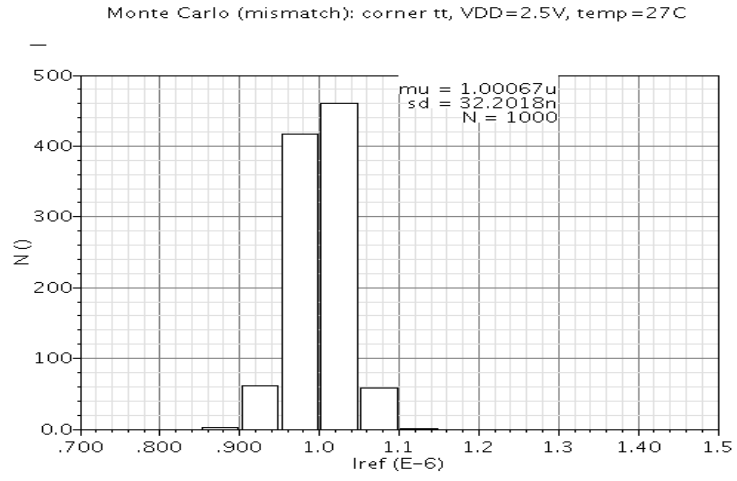

Fig. 6 – Influence of device mismatches on the current reference.

The rejection of the supply voltage is illustrated in Fig.7. At low frequencies the value of PSRR is about –164 dB; it gives the line sensitivity shown in Fig. 4. PSRR decreases below –180 dB at frequencies more than 1 MHz due to the filter P_{10} – C inserted in the output stage.

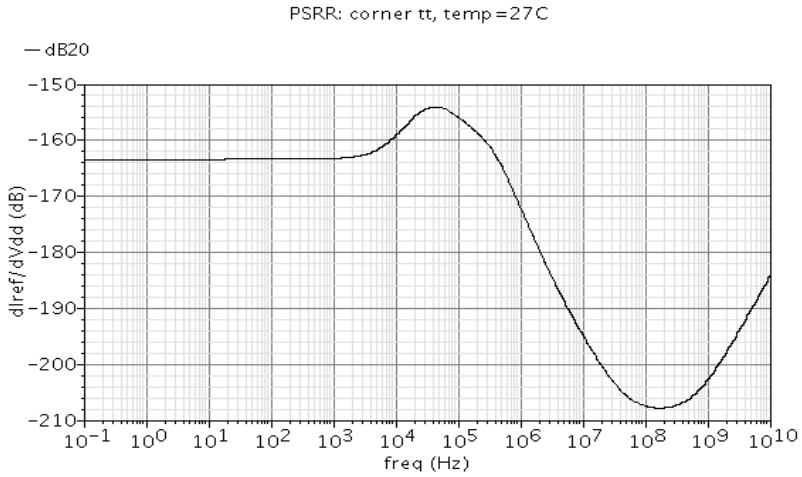

Fig. 7 – PSRR (power supply rejection rate).

The behavior of the circuit in Fig. 1 to certain supply voltage drops is illustrated in Fig. 8. This transient response shows indirectly a high phase margin of the amplifier from inside the I_{ptc} generator. The start-up stage is very efficient; it forces the differential amplifier to enter quickly the nominal operating regime, without oscillations or overshoots.

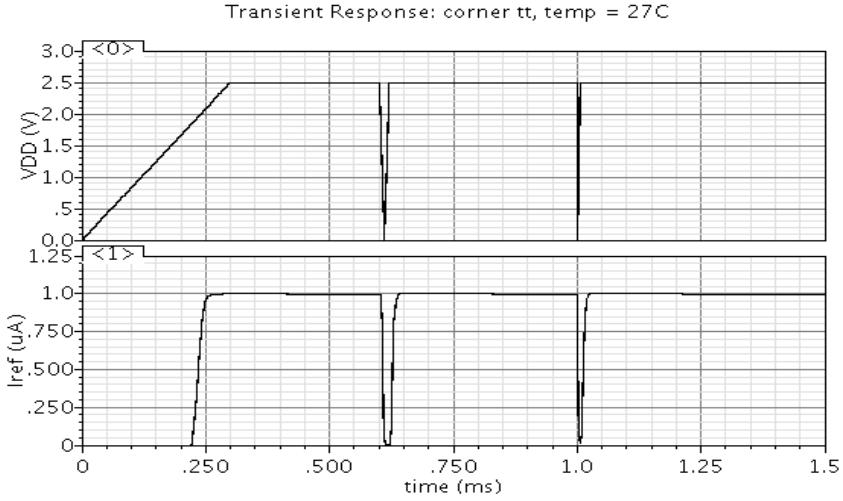

Fig. 8 – Transient response to supply voltage drops.

4. Comparisons with Similar Works

Comparisons between this work and those ones referenced in this paper are listed in the Table 1. The abbreviations "NT" and "T" stand for "no trimming" and "trimming", respectively; the abbreviations "std" and "SOI" are used for "standard" and "silicon on insulator", respectively.

The performances of the current reference described in this paper are comparable with those presented in (Imbrea *et al*., 2013) and are superior to those presented in the other references. In order to decrease the line sensitivity of the proposed circuit it is mandatory to improve PSRR at low frequencies. This parameter is mainly determined by I_{ptc} and I_{ntc} generators.

When comparing values of line sensitivity (row 5 in the table 1), we have to take also into account the values of reference current. For example, one may say in case of this work that the voltage supply variation involves a change of 0.87%/V in the output current I_{ref}.

Table 1
Comparisons

	This work	Imbrea *et al*., 2013	De Vita *et al.*, 2007	Falconi *et al*., 2007
Process	65 nm CMOS std.	65 nm CMOS std.	0.35 µm CMOS std.	0.13 µm CMOS std.
Supply voltage	[2.2, 2.8] V 2.5 V nominal	[2.1, 3.0] V 2.5 V nominal	[2.0, 4.0] V 3.0 V nominal	[0.8, 2.0] V 1.5 V nominal
Reference current	1 µA	1 µA	9.14 nA	10 µA
Line sensitivity	8.7 nA/V	0.5 nA/V	5.6 pA/V	–
Temperature coefficient	12.9 ppm/ºC	11 ppm/ºC	44 ppm/ºC	2.2 %/ºC
Temperature range	[–25, +130] ºC	[–40, +130] ºC	[0, +80] ºC	[–10, +80] ºC
Process sensitivity	Simulated	Simulated	Measured	Simulated
– mismatch (sd/mu)	3.23%	1.53%	–	–
– corners	43% (NT) 0.06% (T)	30% (NT) 0.036% (T)	–	–
– total	–	–	2.16% (NT)	31% (NT)
PSRR @100Hz	–164 dB	–200 dB	–	–

Table 1
Comparisons (continued)

	This work	Quemada *et al.*, 2012	Zhao *et al.*, 2012	Liu *et al.*, 2010
Process	65 nm CMOS std.	0.18 µm CMOS SOI	0.18 µm CMOS std.	0.18 µm CMOS std.
Supply voltage	[2.2, 2.8] V 2.5 V nominal	– 1.5 V nominal	– 1.8 V nominal	[2.0, 3.0] V 2.0 V nominal
Reference current	1 µA	21.1 µA	4.2 µA	10 µA
Line sensitivity	8.7 nA/V	–	–	0.3 µA/V
Temperature coefficient	12.9 ppm/ºC	16.5 ppm/ºC	273 ppm/ºC	170 ppm/ºC
Temperature range	[–25, +130] ºC	[+20, +130] ºC	[–10, +100] ºC	[–20, +120] ºC
Process sensitivity	Simulated	Simulated	Simulated	Simulated
– mismatch (sd/mu)	3.23%	–	–	–
– corners	43% (NT) 0.06% (T)	38% (NT)	33% (NT)	–
– total	–	–	–	2.14% (NT)
PSRR @100Hz	–164 dB	–	–	–

5. Conclusions

The current reference described in this work is built only with regular MOS transistors and vertical substrate PNP transistors; no on-chip resistors or external components are used. The circuit is designed in 65 nm CMOS standard process but can be implemented in any other one. The process variations and device mismatches can be compensated by trimming the sizes of four transistors. Simulations show that the generated current of 1 µA is very weakly sensitive to temperature and voltage supply variations.

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REFERINȚĂ DE CURENT CMOS FĂRĂ REZISTORI

(Rezumat)

Se prezintă un circuit CMOS fără rezistori, care generează un curent de referință cu valoarea 1 µA ± 1 nA în gama de temperatură [–25º, +130]ºC. Curentul de referință se obține prin sumarea a doi curenți care au coeficienți de temperatură pozitiv şi respectiv negativ. Tensiunea de alimentare este 2.5 V ± 12%.

Caracteristicile principale ale referinței de curent propuse sunt coeficientul de temperatură 12.9 ppm/ºC, sensibilitatea 8.7 nA/V la tensiunea de alimentare şi rejecția variațiilor de pe linia de alimentare de –164 dB la frecvențe mici.

Influența variațiilor procesului tehnologic asupra curentului de referință pot fi compensate prin ajustarea dimensiunilor a patru tranzistoare. Simulările de tip Monte Carlo arată o dispersie de 32.2 nA a curentului de referință datorită neîmperechierilor dintre tranzistoare.