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A CMOS OSCILLATOR WITH LOW SENSITIVITY TO PROCESS, SUPPLY VOLTAGE AND TEMPERATURE

BY

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Abstract. The paper presents the design of a 100 kHz relaxation oscillator without external components. The circuit is implemented in CMOS 65 nm standard process and contains only MOS transistors. It operates with supply voltage in the range [2.2… 2.8] V from –30°C to +130°C. The oscillation frequency has low sensitivity to process variations, supply voltage and temperature. The process corners cause frequency variations of ± 0.65% compared to the typical one. Changing the supply voltage from 2.5 V (nominal value) will decrease the oscillation frequency with less than 0.093%. The frequency drift due to the temperature is ± 0.006% in the range [–10 ... +130]°C, which means a temperature coefficient of 0.85 ppm/ºC. The quiescent current of the circuit is less than 1.5 µA.

Key words: CMOS circuit; relaxation oscillator; process corner; PVT sensitivity.

1. Introduction

Several topologies of relaxation oscillators have been proposed. The circuit architecture sketched in Fig. 1 is based on current and/or voltage reference circuits; it underlies the oscillator described in this paper.

The current I is used for charging and discharging the capacitor C

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between two threshold voltages (high and low) denoted by V_{TH} and V_{TL}. In this case, a duty cycle of 50% is intended for the output signal (it is usual derived from one of the latch outputs Q or QN and it is not shown in Fig. 1). If the capacitor *C* is charged and discharged by two currents having different values then the duty cycle is more or less than 50%. The end of the charging (discharging) period and start of the discharging (charging) period are decided by means of the voltage comparator compH (compL) and the SR-latch.

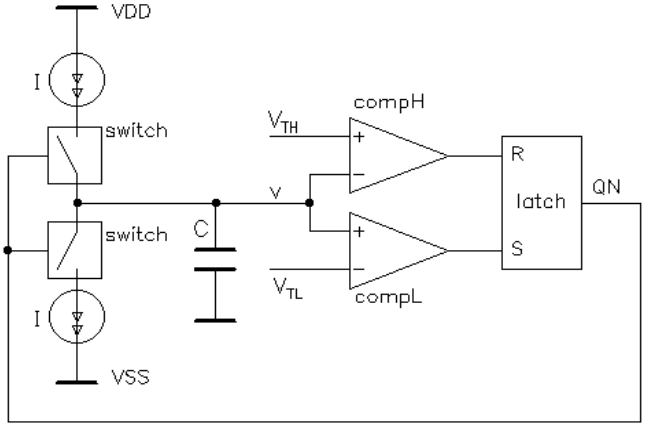

Fig. 1 – Relaxation oscillator based on current/voltage references.

Assuming that *I*, *C*, V_{TH} and V_{TL} are constants and the comparators have zero offset voltages, the oscillation frequency is given by

$$f = \frac{I}{2C(V_{TH} - V_{TL})}. \tag{1}$$

The voltage *v* increases and decreases linearly in time across capacitor *C*. By differentiating the above equation it follows that

$$\frac{df}{f} = \frac{dI}{I} - \frac{dC}{C} - \frac{d(V_{TH} - V_{TL})}{V_{TH} - V_{TL}}. \tag{2}$$

Every term (relative variation) in eq. (2) depends on the technological process, supply voltage and temperature; these three disturbing factors are usually abbreviated as PVT. The last term in eq. (2) includes offset voltages of the two comparators. Also, the switching errors are included in d*I*/*I*.

The oscillators described in the references mentioned in this paper differ from the one in Fig. 1 in many aspects.

In (Denier, 2010) only one current mode comparator is used instead of two voltage comparators; it compares the voltage across a capacitor with a reference voltage proportional to the thermal voltage. The capacitor is charged

by a PTAT (proportional to absolute temperature) current and abruptly discharged. The digital part is supplied from a voltage regulator.

A current proportional to emitter-base voltage V_{EB} of a bipolar transistor charges the capacitor of the oscillator proposed by Radoias *et al*., (2011). The capacitor is abruptly discharged. Only one current comparator is used. A flip-flop ensures a 50% duty cycle output signal.

The circuit proposed by Soldera *et al*., (2012), does not require reference voltages; the analog comparison is based on the threshold voltage of two NMOS transistors. A floating capacitor is alternately charged with equal but opposite CTAT (complementary to absolute temperature) currents.

The oscillator presented by Paidimarri *et al*., (2013), includes a voltage comparator with offset cancellation and a Schmitt trigger. Two capacitors, one resistor and a PTAT current reference are also used.

A simple bias circuit that produces a reference current and a low reference voltage, based on diffused and polysilicon resistors is used by Tsubaki *et al*., (2013). The voltage comparators are compensated for offset voltage and delay time. To control and compensate for oscillation frequency characteristics, a digitally controlled technique is used.

The architecture of the oscillator proposed by Taha *et al*., (2014), is close to that in Fig. 1. In order to eliminate the temperature dependency of the comparator delay, the comparators have been replaced with high speed common-source stages followed by inverters. A bandgap circuit is used. The oscillation frequency can be digitally trimmed.

2. Circuit Description

The circuit in Fig. 2 is a direct implementation of the architecture shown in Fig. 1. It does not contain any offset compensation and trimming capabilities.

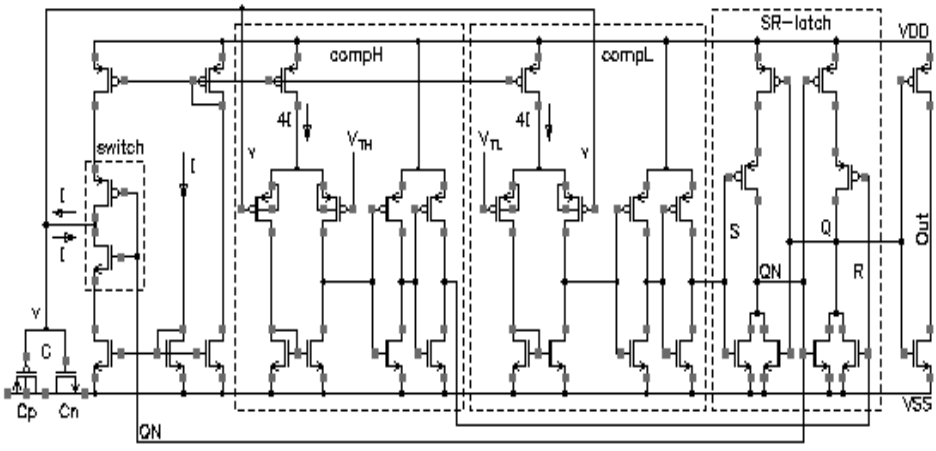

Fig. 2 – Implementation of the relaxation oscillator.

Comparators compH and compL are identical and generate the pulses S (Set) and R (Reset) for the SR-latch; each comparator includes a differential amplifier and two inverters. The transistors are sized so that the pulses S and R are as small as possible, depending on process variations (corners). PMOS differential pairs are chosen to avoid body effect.

Generally, comparators require high bias currents to have small response time. However, the bias current of the comparators in Fig. 2 (denoted by 4*I*) is only 600 nA, which represents a very small value.

The capacitor *C* consists of two normal 2.5 V transistors, NMOS and PMOS, designed to compensate for the oscillation frequency to process variations.

The switch must be fast to minimize switching errors; it includes two small size transistors driven by the latch output QN.

The current *I* and the threshold voltages V_{TH}, V_{TL} are obtained from reference circuits (not shown here) similar to those presented by Imbrea *et al*., (2013) and Imbrea *et al*., (2011). Only a few branches have to be added to the N or P mirrors in the current generators in order to obtain a bias current for the oscillator. The temperature characteristics of this current can be adjusted according to those of the capacitor *C*. Furthermore, it is possible for the capacitor and current changes due to process variations to compensate each other to a certain extent.

Current and voltage reference circuits are often present in the actual electronic systems, so the implementation shown in Fig. 2 becomes very effective from the point of view of silicon area.

The oscillator induces switching noise in the current and voltage reference circuits. However, the current mirrors and buffers through which the current *I* and threshold voltages V_{TH}, V_{TL} are obtained greatly reduce this noise, as will be shown in the next section.

3. Simulation Results

Some characteristic signals of the oscillator operation are illustrated in Fig. 3. The difference between V_{TH} and V_{TL} is about 200 mV. The capacitor *C* is charged and discharged by less than 150 nA in the entire temperature range. The quiescent current I_{DD} does not exceed 1.5 µA. In switching regime the current consumption from the power supply increases much but its root mean square is only 21 µA.

The output signal denoted by *Out* has approximately 160 ps rise time and 60 ps fall time. The load connected to *Out* is an inverter (not represented in Fig. 2).

Temperature dependence of the oscillation frequency is shown in Fig. 4. The relative variation is 0.25% but in the temperature range [–10… +130] ºC it is only ±0.006% which means about 0.86 ppm/ ºC.

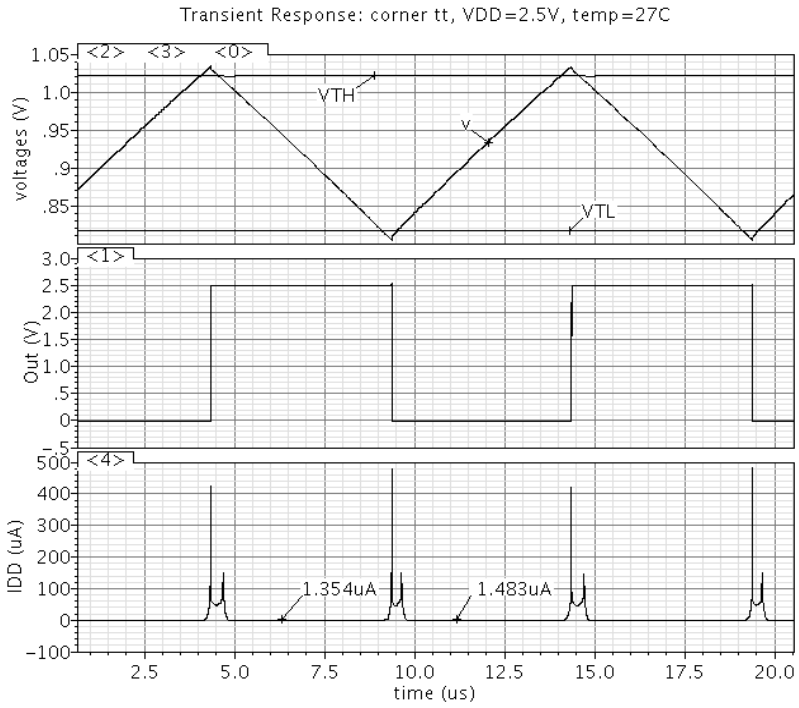

Fig. 3 – Specific signals of the oscillator of Fig. 2.

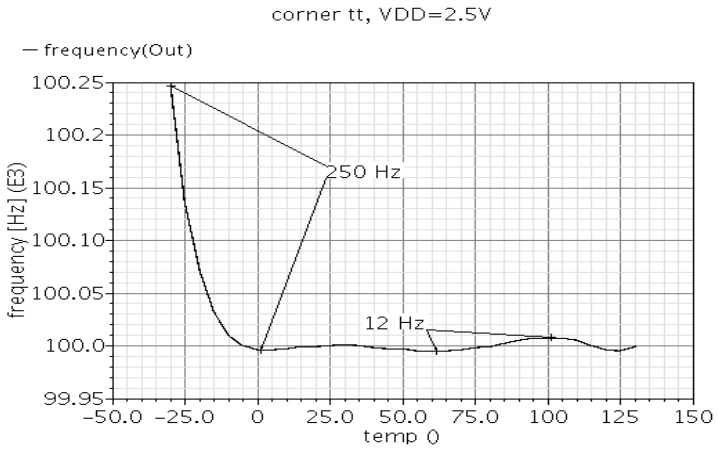

Fig. 4 – Oscillation frequency versus temperature.

The influence of the supply voltage V_{DD} on oscillation frequency is shown in Fig.5. If V_{DD} changes between 2.2 V and 2.8 V, which means 2.5 V ± ± 12%, then the frequency decreases with about 93 Hz from the nominal value (*i.e.*, –0.093%). This also means a line sensitivity of 155 Hz/V or 0.15 %/V.

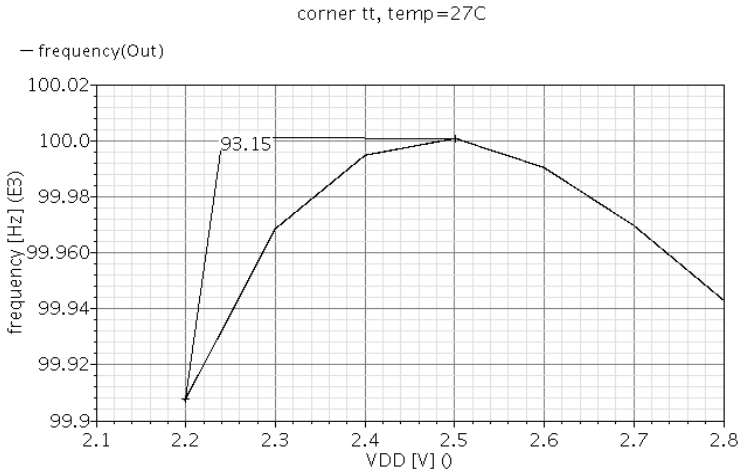

Fig. 5 – Oscillation frequency versus supply voltage.

The influence of process variations (corners) on the oscillation frequency is shown in Fig. 6. The extreme corners are sf (slow N, fast P) and fs (fast N, slow P). Frequency changes are within ±0.65% compared to typical corner tt.

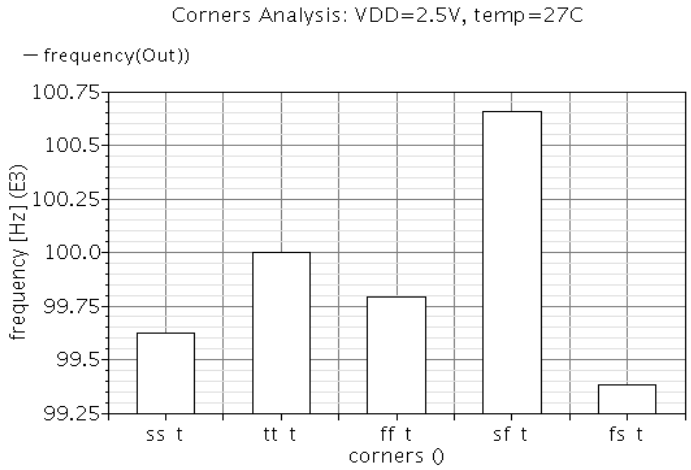

Fig. 6 – Oscillation frequency versus process corners.

As shown in the previous three figures, the oscillator has low PVT sensitivities. This means that the relative variations in eq. (2) compensate each other very well.

The mismatch between devices also affects the oscillation frequency. Monte Carlo simulations that include only mismatch are shown in Fig. 7. Some correlations between transistor parameters were considered. The ratio *standard deviation/mean* (sd/mu) of the oscillation frequency is 11%. This value is

relatively high and is mainly due to the offset voltages of the comparators. It is the main disadvantage of the presented circuit. By using offset cancellation techniques we may greatly reduce the mismatch effects.

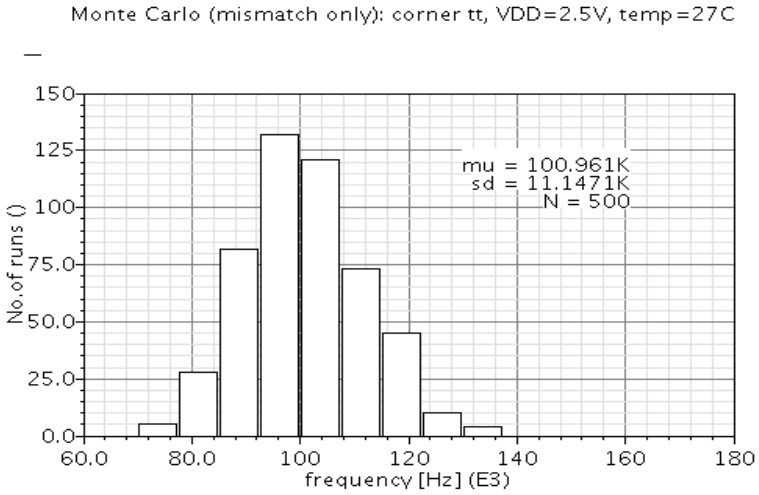

Fig. 7 – Mismatch influence on oscillation frequency.

The switching noise induced by the oscillator in the reference circuits is illustrated in Fig. 8. I_{ntc}, I_{ptc} and V_{ref} denote the currents with negative/positive temperature coefficient and the reference voltage, respectively. The levels of noise are very low, namely 3.5 ppm, 0.15 ppm and 0.58 ppm.

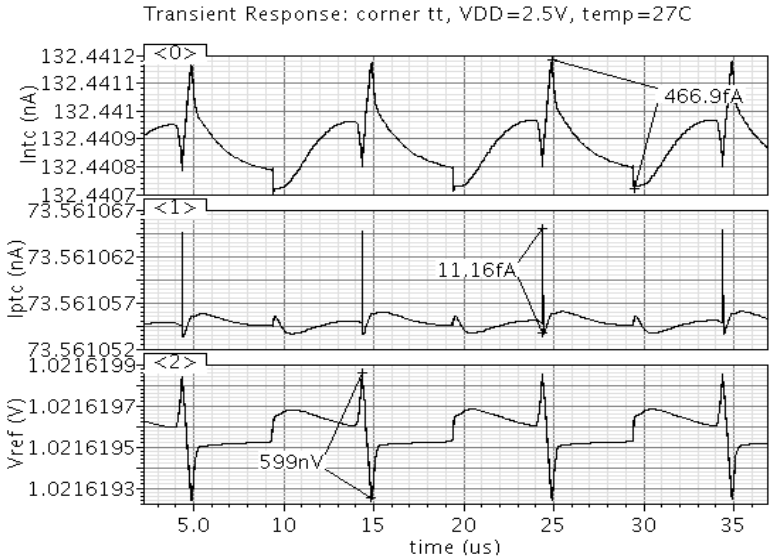

Fig. 8 – Noise induced in the current/voltage reference circuits.

4. Comparisons with Similar Works

Comparisons between this work and those referenced in this paper are listed in the Table 1.

Table 1
Comparisons

	This work	Denier 2010	Radoias *et al.*, 2011	Soldera *et al.*, 2012
technological process	65 nm CMOS std.	0.35 µm CMOS std.	- BiCMOS	0.5 µm CMOS std.
supply voltage	[2.2, 2.8] V 2.5 V nominal	[1.0, 3.6] V –	[2.0, 5.0] V 3.0 V nominal	[1.5, 5.5] V –
osc. frequency	100 kHz	3.3 kHz	100 kHz	tens of kHz
V sensitivity	0.15 %/V	3.5 %/V	–	±1.9 %/V
T sensitivity	0.86 ppm/ºC	500 ppm/ºC	737 ppm/ºC	267 ppm/ºC
temp. range	[-10, +130] ºC	[-20, +80] ºC	[-40, +150] ºC	[-40, +125] ºC
P sensitivity – mismatch (sd/mu) – corners – total	Simulated 11 % ±0.65% –	Measured – – 6.9 %	–	–

Table 1
Comparisons (continued).

	This work	Paidimarri *et al.*, 2013	Tsubaki *et al.*, 2013	Taha *et al.*, 2014
technological process	65 nm CMOS std.	65 nm CMOS std.	0.18 µm CMOS std.	65 nm CMOS std.
supply voltage	[2.2, 2.8] V 2.5 V nominal	– 1.0 V nominal	[1.0, 1.8] V –	[1.4, 1.9] V –
osc. frequency	100 kHz	18.5 kHz	32.55 kHz	157 MHz
V sensitivity	0.15 %/V	1 %/V	1.1 %/V	3.2 %/V
T sensitivity	0.86 ppm/ºC	38.5 ppm/ºC	120 ppm/ºC	171.4 ppm/ºC
temp. range	[–10, +130] ºC	[–40, +90] ºC	[–40, +100] ºC	[–20, +120] ºC
P sensitivity – mismatch (sd/mu) – corners – total	Simulated 11 % ±0.65% –	–	Measured – –1.39%	–

Note that the oscillators described by Denier, (2010), Soldera *et al.*, (2012) and Tsubaki *et al.*, (2013), were fabricated and the PVT sensitivities were measured after a trimming operation. Also, the oscillators described by Radoias *et al.*, (2011) and Paidimarri *et al.*, (2013) were measured after fabrication but do not contain trimming capabilities.

5. Conclusions

The relaxation oscillator described in this work is built only of normal 2.5 V MOS transistors; no on-chip resistors or external components are used. The circuit is designed in 65 nm CMOS standard process and supplied from 2.5V nominal value. The oscillator architecture is based on current/voltage reference circuits.

Simulations show that the frequency of the output signal is very weakly sensitive to temperature, voltage supply and process corners. Instead, device mismatches have a greater influence on the oscillation frequency. The switching noise induced by the oscillator in the reference circuits is quite small. The quiescent supply current is less than 1.5 µA.

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OSCILATOR CMOS CU SENSIBILITATE MICĂ LA PROCES, TENSIUNE DE ALIMENTARE ŞI TEMPERATURĂ

(Rezumat)

Se prezintă un oscilator de relaxare CMOS fără rezistori sau componente exterioare chip-ului şi care generează o tensiune dreptunghiulară cu frecvenţa de 100 kHz. Circuitul are o arhitectură bazată pe referinţe de curent şi de tensiune. Tensiunea de alimentare este 2.5 V ± 12% iar gama temperaturilor de operare este [–30º, +130] ºC.

Caracteristicile principale ale oscilatorului prezentat sunt: 0.86 ppm/ºC coeficient de temperatură, 0.15 %/V sensibilitate la tensiunea de alimentare şi ±0.65% variaţie relativă la procesul tehnologic (cornere) ale frecvenţei de oscilaţie. O influenţă mai mare asupra acesteia o au neîmperechierilor dintre tranzistoare, raportul dintre deviaţia standard şi medie fiind de aproximativ 11%.

Nivelurile de zgomot induse de către oscilator în circuitele de referinţă care sunt utilizate pentru obţinerea curentului de polarizare şi ale tensiunilor de prag sunt foarte mici. De asemenea, consumul static de current de la sursa de alimentare este de aproximativ 1.5 µA.