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LINEAR VOLTAGE-TO-CURRENT CONVERTER WITH SMALL AREA

BY

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Abstract. A linear CMOS circuit without resistors that converts an input voltage up to 5 MHz frequency into an output current with high accuracy is presented. The circuit is designed in 65 nm CMOS standard technology and operates in the temperature range [–30, +130] °C with supply voltage from 2.2 V to 2.8 V. The input voltage range is [0.45, 1.75] V; the corresponding output current varies between 30 µA and 100 µA (approximately) in the typical corner. The relative linearity error is between the limits ±0.1% over almost entire range of the input voltage at 1 MHz frequency. The output current depends on temperature and process variations but it keeps strongly the linearity versus input voltage. The silicon area occupied by the circuit is less than 224 μm^2.

Key words: linear circuit; linearity error; power supply rejection rate; voltage-to-current converter.

1. Introduction

Two different approaches of obtaining voltage-to-current converters are illustrated in Fig. 1. In both cases the conversion of the input voltage V_{in} into the output current I_{out} is carried out by means of a polysilicon resistor R; V_{in} can be a constant or variable voltage. The cells named “opamp” and “OA” are high-gain voltage amplifiers.

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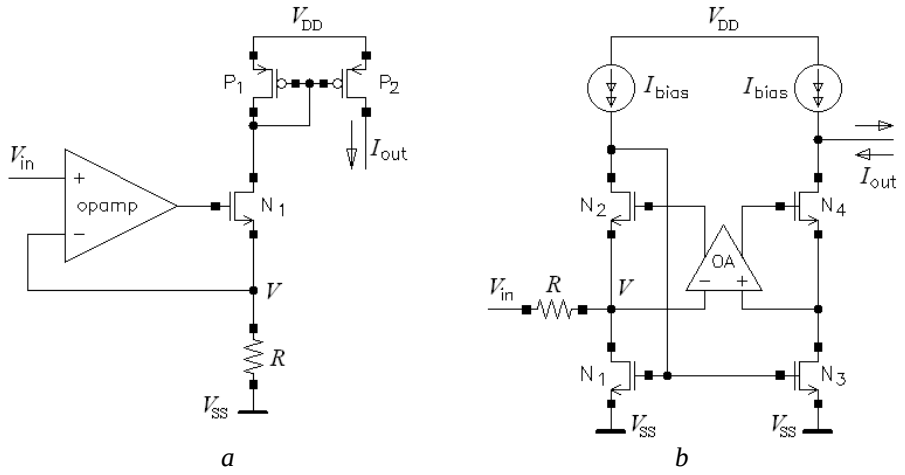

Fig. 1 – Voltage-to-current conversion principles.

The equation underlying the circuit in Fig. 1 *a* is

$$I_{out} = \frac{V}{R} \cong \frac{V_{in}}{R}. \tag{1}$$

It was assumed that transistors P_1 and P_2 have identical sizes. Otherwise, the mirroring factor W_2L_1/W_1L_2 should be considered in eq. (1), where W and L are the channels width and length.

The output current produced by the circuit in Fig. 1 *b* is given by

$$I_{\text{out}} = \frac{V_{\text{in}} - V}{R}, \tag{2}$$

where the voltage V is close to a constant. The transistors N_1 and N_3 have identical sizes; this also applies to N_2 and N_4.

There are certain operational limitations related to the circuits in Fig. 1. When V_{in} decreases to V_{SS} or increases to V_{DD} the conversion errors grow increasingly more. Also, the errors increase with increasing the frequency of V_{in} mainly due to lower gain of the amplifiers.

An ideal conversion means generating an output current that is linear as function of input voltage and also completely independent of the process variations, supply voltage and temperature. In order to reduce the temperature dependence of I_{out}, the polysilicon resistor R can be made of two pieces that have positive and negative temperature coefficients, $R = R_N + R_P$. Even so, the process variations may change R up to 30%.

Voltage-to-current converter circuits based on current-mirror topologies similar to that in Fig. 1 *b* were presented in Srinivasan *et al*., (2005), Hassen *et al*., (2011), Laajimi *et al*., (2012).

The circuit described in Fotouhi, (2001), is derived from the one shown in Fig. 1 *a*. The polysilicon resistor *R* is replaced twice by NMOS transistors, one operating in triode region and the other in saturation region. The drain currents in each of these transistors are nonlinear functions of the input voltage but their sum is linear over a wide input range.

A high-linearity CMOS transconductor based on differential structures without resistors, also derived from the circuit in Fig. 1 *a*, is presented in Lo *et al.*, (2011).

Other circuit topologies, different from those in Fig.1 have been proposed. The transconductor presented in Szczepanski *et al.*, (1993), has a structure formed by cross-coupled differential pairs and a current mirror.

The converter proposed here generates the output current by adding two nonlinear currents as functions of input voltage. The method is the same as that used in Fotouhi, (2001), but the implementation is different, silicon area being reduced by more than 96,000 times.

2. Circuit Description

The schematic of the voltage-to-current converter is shown in Fig. 2.

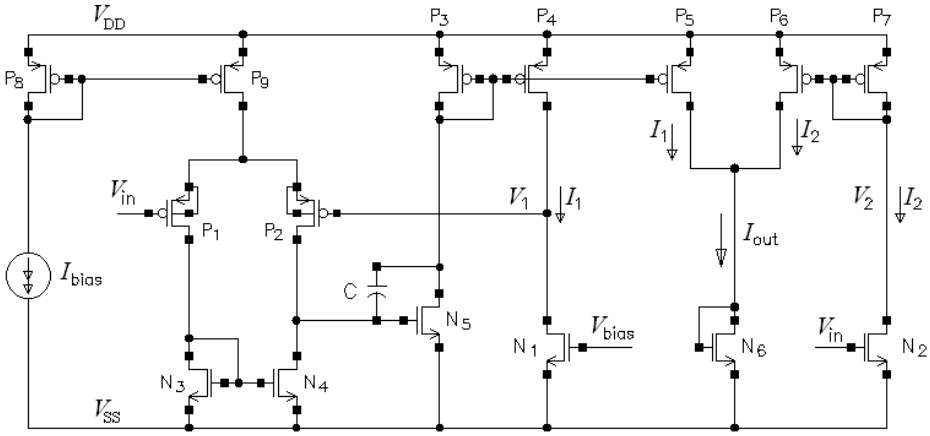

Fig. 2 – Schematic of the proposed voltage-to-current converter.

NMOS transistor N_1 is the load of a two-stage amplifier. The first stage contains a differential pair P_1-P_2 with active loads N_3-N_4, biased via P_8-P_9 mirror. The second stage consists of N_5 and the mirror P_3-P_4. Frequency compensation is done using a small value capacitor C. N_1 is supposed to operate in triode region. This requires that its dimensions are chosen correctly and the gate voltage V_{bias} is close to V_{DD}. In this case, the amplifier will keep the voltage V_1 very close to V_{in}.

This part of schematic described above works just like the circuit in

Fig. 1 *a*; the triode N_1 in Fig. 2 replaces the resistor *R* in Fig. 1 *a*. Note that this amplifier configuration allows a higher conversion range of input voltage. Only the maximum value of V_{in} is limited, which is imposed by the operation of N_1 in the triode region.

NMOS transistor N_2 works in the saturation region. To obtain the square- law behaviour for N_2, V_{in} must not fall below a certain value. This minimum value is close to the threshold voltage. Also, the channel of N_2 must be long enough in order to prevent the channel-length modulation effect; thus, the current through N_2 becomes independent of the drain voltage V_2.

Eqs. (3) and (4) describe the operation of the transistors N_1 and N_2; μ_n, C_{ox}, W/L, V_{thn0} are, respectively, the mobility of electrons, the gate-oxide capacitor per unit area, the channel width/length ratio and the threshold voltage with V_{BS} = 0 V (body-source voltage).

$$I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}\left[2(V_{bias} - V_{thn0})V_1 - V_1^2\right] \cong \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}\left[2(V_{bias} - V_{thn0})V_{in} - V_{in}^2\right], \quad (3)$$

$$I_2 = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}(V_{in} - V_{thn0})^2. \quad (4)$$

As suggested in Fig. 2, P_4 and P_5 must have identical size; the same is true for P_6 and P_7. Assuming $W_1/L_1 = W_2/L_2 = W/L$, it follows that

$$\begin{cases} I_{out} = I_1 + I_2 \cong \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{thn0}^2 + \mu_n C_{ox}\frac{W}{L}(V_{bias} - 2V_{thn0})V_{in} = I_{res} + GV_{in}; \\ I_{res} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{thn0}^2; \\ \frac{\partial I_{out}}{\partial V_{in}} = G = \mu_n C_{ox}\frac{W}{L}(V_{bias} - 2V_{thn0}). \end{cases} \quad (5)$$

The output current I_{out} has two components, namely a "residual" current I_{res} and a useful part GV_{in}. Both I_{res} and transconductance *G* decrease with increasing temperature and depend on process variations. The influence of supply voltage on I_{out}, mainly coming from V_{bias}, can be reduced to low levels.

The transconductance *G* can be compensated for temperature and process to a certain extent through the bias voltage V_{bias}. However, these dependencies may be advantageous in some applications.

For DC and low-frequency applications, the circuit in Fig. 2 can be slightly modified to extend the input voltage range, as shown in Fig. 3. PMOS transistor P_{10} shifts up the gate voltage of N_2 and thus V_{in} may decrease down to V_{SS}; P_{10} operates in the subthreshold region. Eq. (4) becomes

$$I_2 = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}(V_{in} + V_{SG10} - V_{thn0})^2 \approx \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}V_{in}^2. \quad (6)$$

By choosing the appropriate size for P_{10} and a small bias current I_b, the voltages V_{SG10} and V_{thn0} may cancel each other.

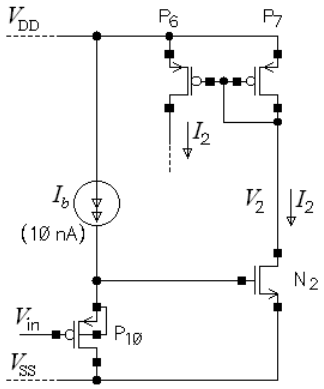

Fig. 3 – Increasing the conversion range of input voltage.

Substituting (6) in (5) we get

$$\begin{cases} I_{out} = I_1 + I_2 \approx \mu_n C_{ox} \dfrac{W}{L}(V_{bias} - V_{thn0})V_{in} = GV_{in}; \\ \dfrac{\partial I_{out}}{\partial V_{in}} = G = \mu_n C_{ox} \dfrac{W}{L}(V_{bias} - V_{thn0}). \end{cases} \tag{7}$$

In this case, the residual current is very close to zero over a wide range of temperature and also in all process corners. Unfortunately, the solution depicted in Fig. 3 is not valid at high frequencies because the gate voltage of N_2 cannot accurately follow the input voltage V_{in}.

3. Simulation Results

The transient responses to large input signals, which characterize the voltage-to-current converter in Fig. 2, are illustrated in Figs. 4,…,7. The frequency and range of input voltage are 1 MHz, respectively [0.45, 1.75] V.

The absolute and relative linearity errors shown in Fig. 4 are given by eqs. (8), where I_{ideal} is an ideal current with triangular variation in time between the limits of 30 µA and 100 µA.

$$\begin{cases} \text{Abs. error} = I_{out} - I_{ideal}; \\ \text{Rel. error} = \dfrac{I_{out} - I_{ideal}}{I_{ideal}}. \end{cases} \tag{8}$$

From Fig. 5 it can be seen that transconductance G decreases with temperature from 68 µS to 39.5 µS; G (27ºC) = 53.8 µS. The residual current I_{res} changes from 39.5 µA to 19.7 µA; I_{res} (27ºC) = 30 µA.

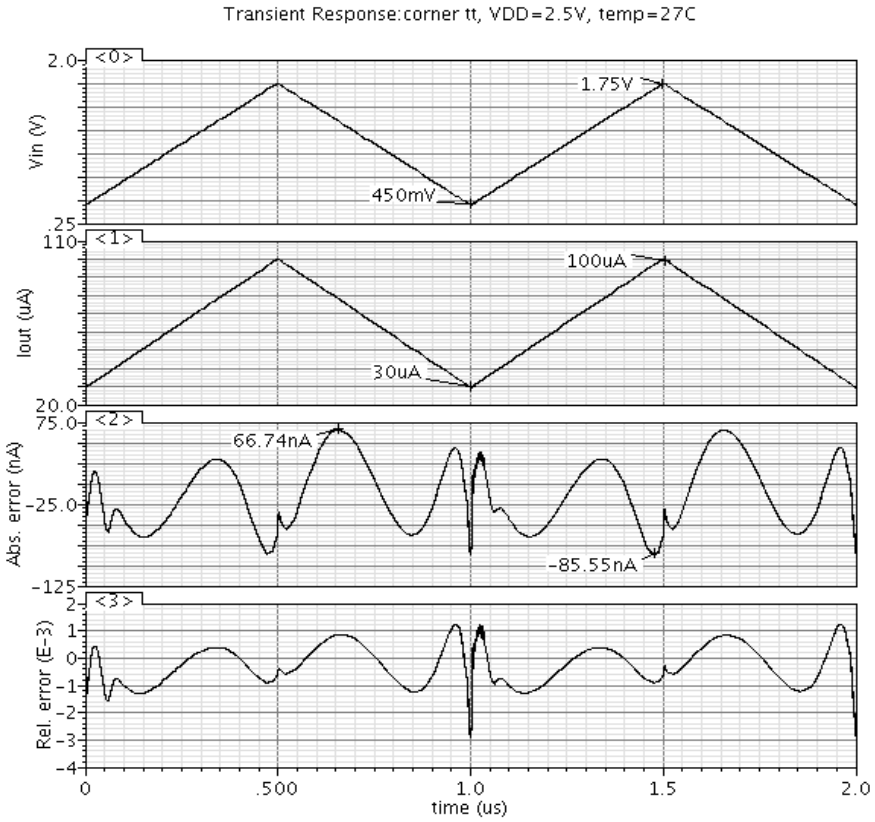

Fig. 4 – I_{out} *versus* V_{in} and linearity errors.

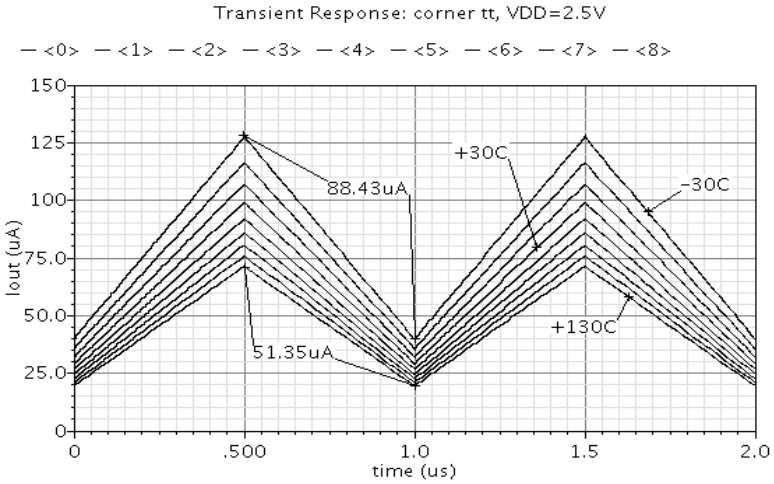

Fig. 5 – Influence of temperature on current I_{out}.

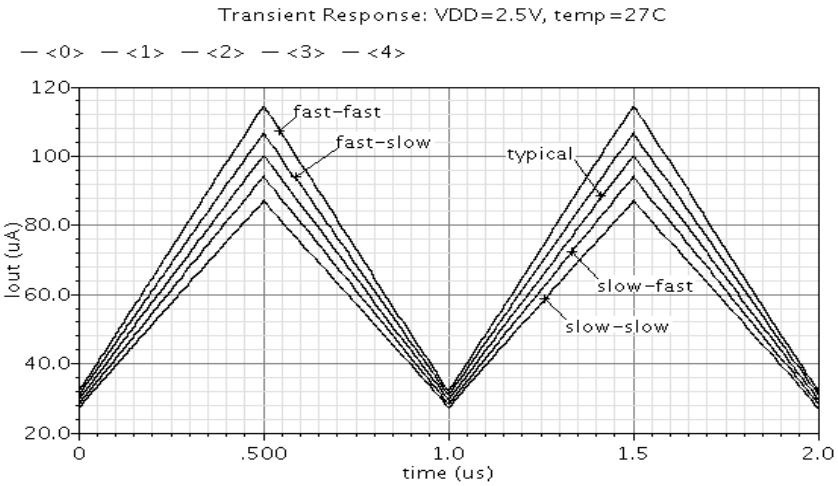

Fig. 6 – Influence of process variations on current I_{out}.

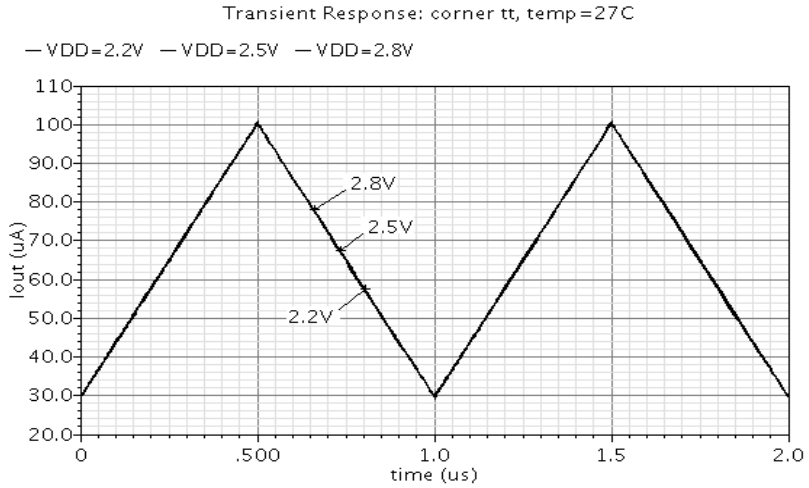

Fig. 7 – Influence of supply voltage on current I_{out}.

Process variations have less influence on G and I_{res} than temperature (Fig. 6). From slow-slow to fast-fast corner, G changes from 46 µS to 63.3 µA and I_{res} changes from 27.27 µA to 32.3 µA.

The supply voltage V_{DD} has small influence on G and I_{res} (Fig. 7); I_{out} has about 850 nA/V line sensitivity. These are true if and only if V_{bias} is isolated from V_{DD}.

The highest current consumption of the circuit occurs in fast-fast corner with 2.8 V supply voltage and it is less than 265 µA. The power supply rejection capability is shown in Fig. 8.

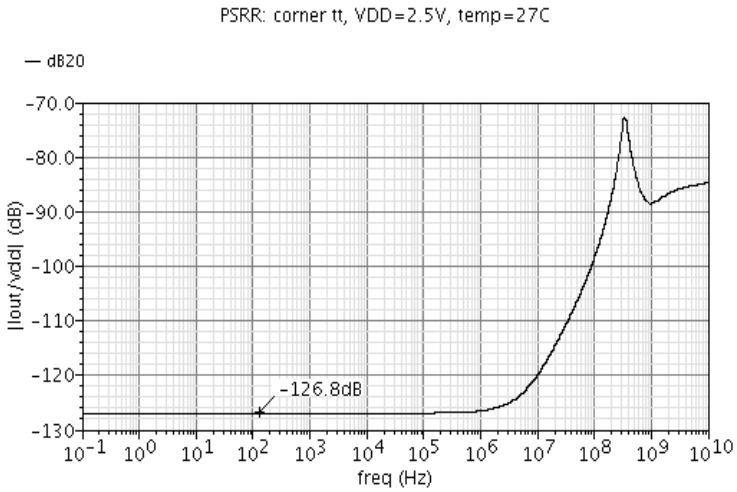

Fig. 8 – Power supply rejection rate.

The layout of the voltage-to-current converter is illustrated in Fig. 9; the silicon area is less than 224 μm^2 (16 µm × 14 µm).

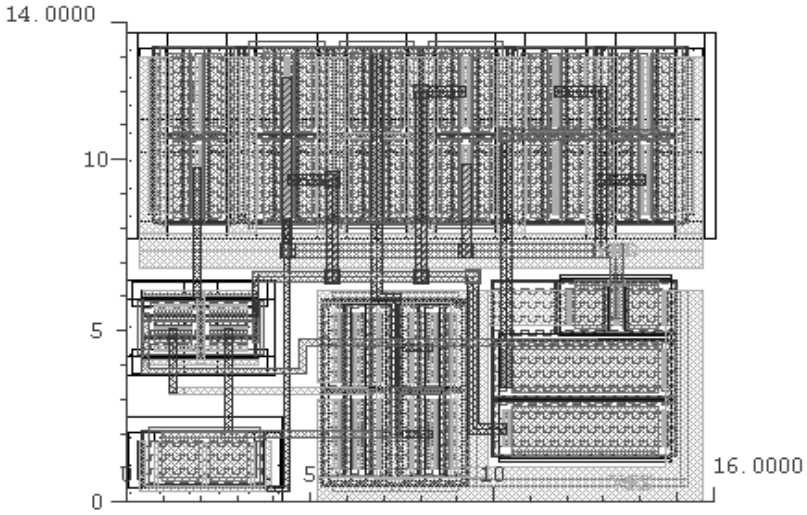

Fig. 9 – Layout of the proposed circuit.

The circuit presented in this paper can be compared with that in Fotouhi, (2001); the method of adding two nonlinear currents as functions of the input voltage is the same. Some comparisons are given in the table below. The most important advantage of the proposed circuit is silicon area. It is considerably less, about (65 nm/600 nm) × (200 mm^2/224 μm^2) = 96,726 times.

Information related to the influence of process variations, temperature and supply line on the output current are not provided in (Fotouhi, 2001).

	This work	Fotouhi 2001
Process	65 nm CMOS std.	0.6 μm CMOS std.
Silicon area	224 μ^2	200 mm^2
Transconductance (typical)	53.8 μS (at 27ºC)	24.7 μS (at 27ºC)
Linearity error (relative)	±0.1%	±0.5%

Fig. 10 shows the transient response of the circuit with increased conversion input range. The sizes of transistors N_1 and N_2 were adjusted to keep the upper limit of 100 μA for the output current. Although the input frequency is lowered to 1 kHz, the linearity errors are 10 times higher compared to those shown in Fig. 4.

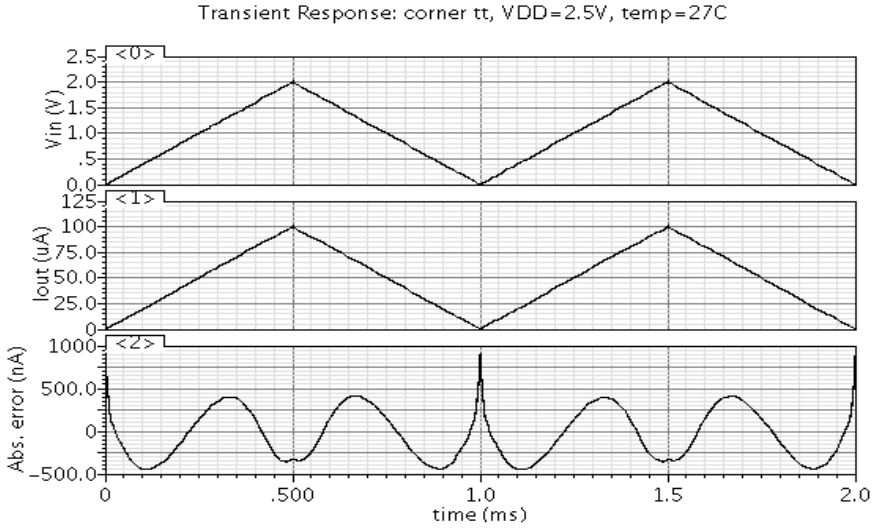

Fig. 10 – Response of modified circuit (Fig. 3).

4. Conclusions

The voltage-to-current converter described in this work is designed in CMOS 65 nm standard process using only MOS transistors. The linearity errors of the output current are in the limits of ±0.1% up to 1 MHz input frequency. The range of the input voltage can be extended from [0.45, 1.75] V to [0, 2.0] V by adding of two PMOS transistors only. The silicon area occupied by the circuit is very small, less than 224 μm^2. The simulations show a low influence of supply voltage on the output current. The process variations and temperature have a greater impact but the output current remains linear as a function of input voltage.

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CONVERTOR LINIAR TENSIUNE-CURENT CU ARIE MICĂ

(Rezumat)

Se prezintă un convertor liniar tensiune-curent care funcționează în intervalul de temperatură [–30º, +130] ºC şi cu tensiuni de alimentare de la 2.2 V până la 2.8 V, valoarea nominală fiind 2.5 V. Circuitul este proiectat într-o tehnologie CMOS standard de 65 nm şi conține numai tranzistoare MOS. Gama de conversie a tensiunii de intrare este [0.45, 1.75] V iar curentul generat este cuprins între 30 μA şi 100 μA. Acesta se obține prin însumarea a doi curenți neliniari în raport cu tensiunea de intrare, generați de două tranzistoare NMOS care funcționează în regim de triodă şi respectiv în regiunea de saturație. Eroarea relativă de liniaritate a curentului de ieşire se păstrează în limitele ± 0.1% până la frecvența de 1 MHz. Variațiile procesului tehnologic şi de temperatură influențează valorile curentului de ieşire însă liniaritatea acestuia nu este afectată. Variațiile tensiunii de alimentare au o influență mică deoarece capacitatea de rejecție a circuitului este mare (–120 dB). Aria de siliciu ocupată este de aproximativ 224 μm^2.

Pentru aplicații de joasă frecvență, gama de conversie a tensiunii de intrare se poate extinde la [0.0, 2.0] V prin introducerea în schema circuitului a numai două tranzistoare PMOS. Erorile absolute de liniaritate se măresc însă de aproximativ 10 ori.