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CMOS SCHMITT TRIGGER WITH CURRENT-CONTROLLED HYSTERESIS

BY

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Abstract. A new topology of Schmitt trigger circuit is proposed; the hysteresis can be adjusted by means of a bias current. The circuit is designed in 65 nm CMOS standard process and operates at 1 V (± 10%) supply voltage in the temperature range [–40, +125] °C. It can be used in both digital and analog applications up to 5 GHz input frequency. The silicon area occupied by the circuit is less than 21 μm^2.

Key words: hysteresis; Schmitt trigger; threshold control; process corners.

1. Introduction

Several configurations of Schmitt trigger circuits have been proposed. Some of them are shown in Fig. 1; all these schematics include enhancement-mode transistors only. The threshold voltages V_{tL} and V_{tH} specific to a Schmitt trigger, also called *Low* and *High switching thresholds*, are dependent on the process variations, supply voltage and temperature. The frequency of the input signal V_{in} also affects V_{tL} and V_{tH} due to the intrinsic parasitic capacitors (not represented in Fig. 1).

Explanations and switching threshold calculations relating to the circuits in Fig. 1 *a*, *b*, *c* can be found in (Dokic, 2012). It can be seen that the

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schematic in Fig. 1 *c* is derived from the one in Fig. 1 *a* by removing two PMOS transistors; a similar way to get another trigger circuit, starting from that in Fig. 1 *a*, is to remove two NMOS transistors.

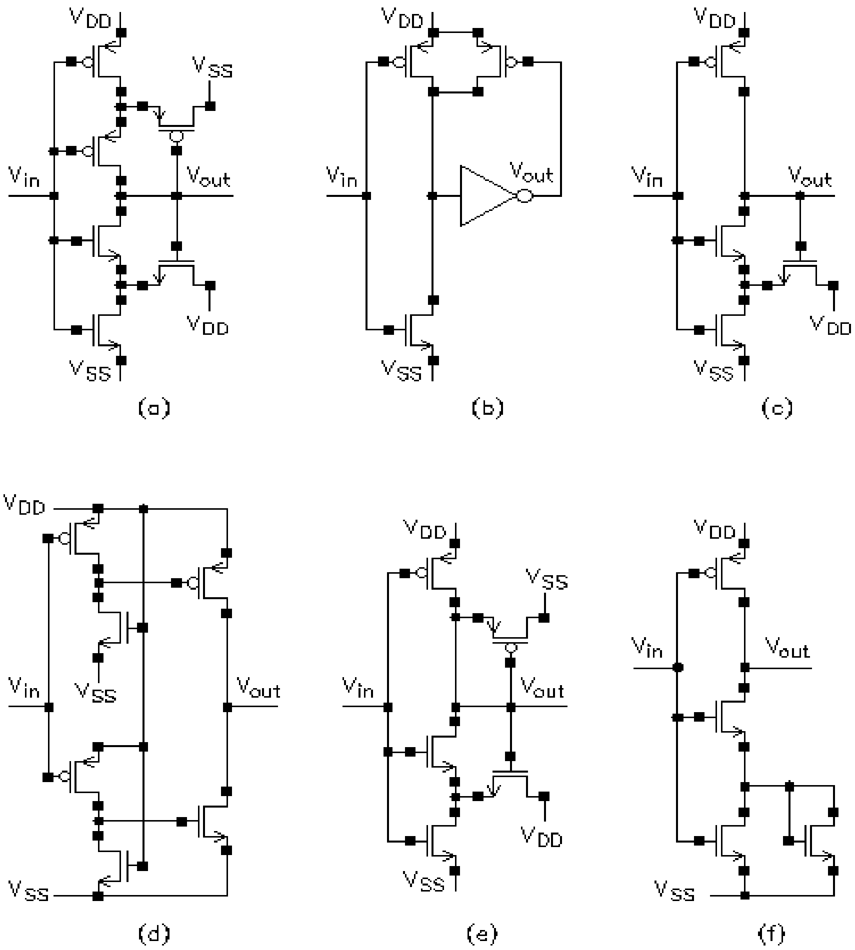

Fig. 1 – Configurations of CMOS Schmitt trigger circuits.

The circuits depicted in Fig. 1 *d*, *e*, *f*) are taken, in this order, from (Madhuri *et al*., 2012; Arith *et al*., 2013; Saxena *et al*., 2014). The last two schematics may also be regarded as derived from that in Fig. 1 *a*, the circuit which is known as "conventional" Schmitt trigger.

The trigger described in (Singhanath *et al*., 2011) is based on dynamic body biasing technique and consists of three stage CMOS inverters. The switching thresholds can be independently adjusted by controlling the body potential.

A differential Schmitt trigger with tunable hysteresis is presented in (Yuan, 2010). The core of this circuit is a cross-coupled inverter pair. The hysteresis (i.e., the difference $V_{tH} - V_{tL}$) can be adjusted by varying the current through symmetrical loads.

The trigger described below has one input and one output, as those in Fig. 1. An external bias current is used to control the hysteresis. To some extent, the bias current is a means to compensate for process variations, supply voltage and temperature.

2. Circuit Description

The schematic of the proposed Schmitt trigger, shown in Fig. 2, contains the inverters N_1–P_1, N_2–P_2 and the current sources P_5 and P_3. The second inverter N_2–P_2 is supplied directly from V_{DD} while the first inverter N_1–P_1 is supplied from the current sources P_5 and P_3. Except for P_4 and P_5 which have long channels, all other transistors have short channels (*i.e.*, minimum or close to the minimum length, specific to core devices), in order to achieve an operating speed as high as possible. The intrinsic capacitors C_1, C_2 do influence the switching thresholds at high frequencies; C_1 and C_2 are mainly gate capacitors and can be approximated by the relations

$$C_1 \approx C_{g\,\mathrm{N2}} + C_{g\,\mathrm{P2}}, C_2 \approx C_{g\,\mathrm{P3}} + C_{Inv} \tag{1}$$

where: C_{Inv} is the input capacitance of the inverter named *Inv*.

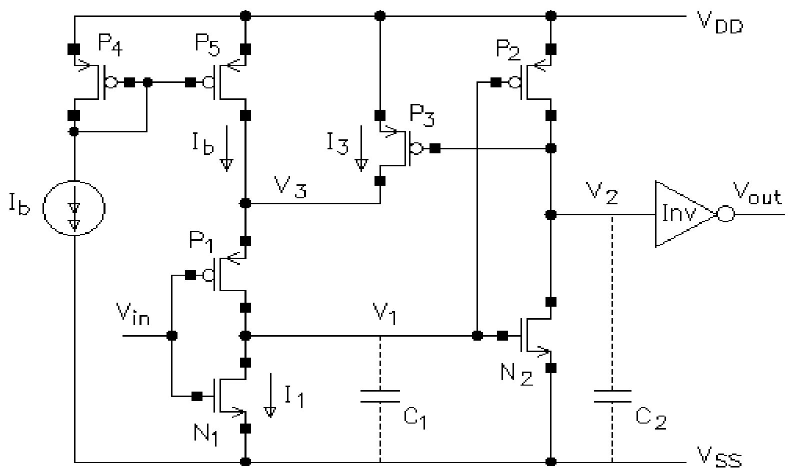

Fig. 2 – Schematic of the proposed Schmitt trigger.

The functional description and calculation of the circuit switching thresholds V_{tL} and V_{tH} will be done by means of the time diagrams illustrated in

Fig. 3; these waveforms are taken from a low-frequency transient simulation.

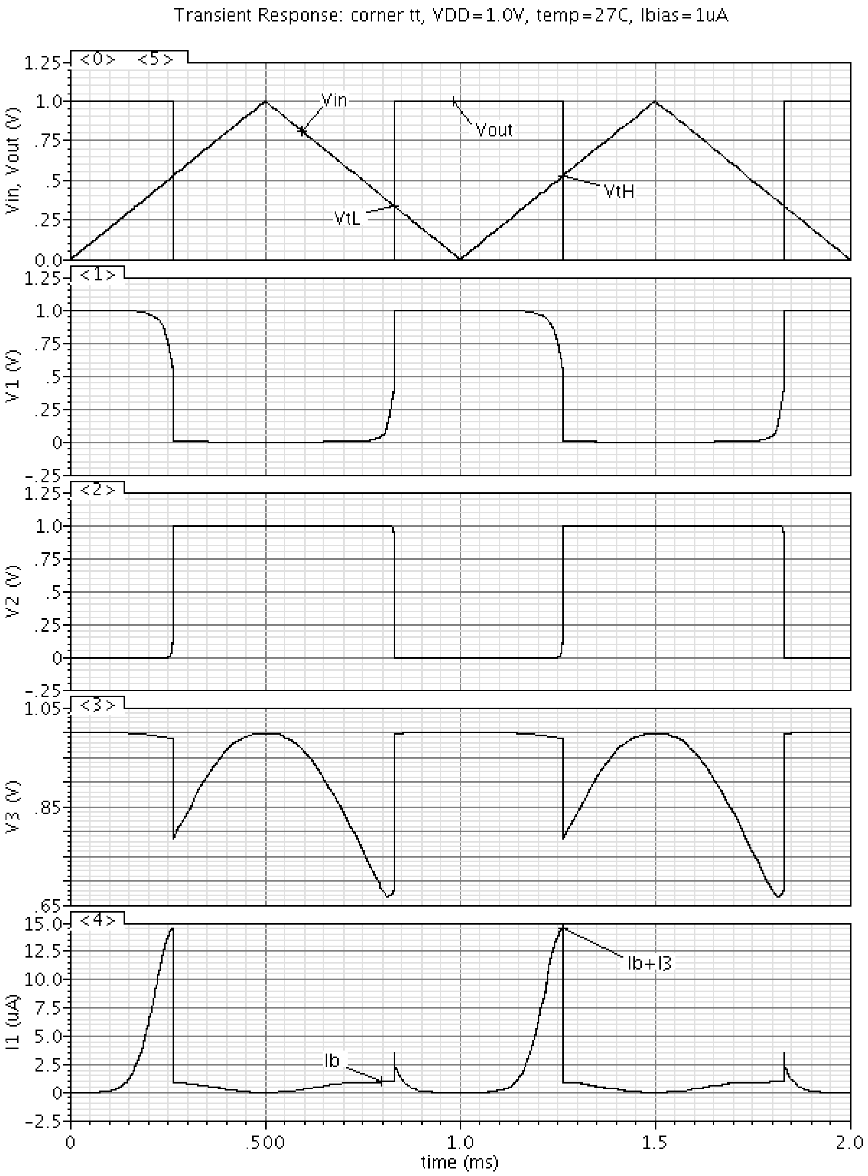

Fig. 3 – Waveforms specific to the proposed Schmitt trigger.

At low values (close to V_{SS}) of the input voltage V_{in} the transistor N_1 is off ($I_1 = 0$); all this time the transistors P_1, P_3, P_5 are working in the triode region at zero drain current and the voltages V_1, V_3 are close to V_{DD}. Increasing V_{in} will determine N_1 to enter the active (or saturation) region, while P_1, P_3 and P_5

remain in the triode region. When V_{in} reaches the high threshold V_{tH}, the transistors P_1, P_3 and P_5 enter the active region. At this moment the current through P_5 is equal to I_b, V_1 falls approximately to 0.5 V and N_1 is still active; also, V_2 reaches about 0.15 V and V_3 drops to about 0.8 V.

From Fig. 2 (at low frequencies) it follows that

$$I_1 = I_b + I_3. \tag{2}$$

For both transistors N_1 and P_3, working in strong inversion, we can evaluate the drain currents by using the square law

$$I_{\mathrm{D}} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(|V_{\mathrm{GS}}| - |V_{\mathrm{th0}}|)^2(1+\lambda|V_{\mathrm{DS}}|), \tag{3}$$

where μ, C_{ox}, W/L, V_{th0} and λ are, respectively, the mobility of charge carriers, the gate-oxide capacitor per unit area, the channel width/length ratio, the threshold voltage with $V_{\mathrm{BS}} = 0$ V (body-source voltage) and the channel-length modulation coefficient.

By combining (2) and (3) we get successively

$$\begin{aligned}&\frac{1}{2}\mu_n C_{oxn}\frac{W_1}{L_1}(V_{tH} - V_{\mathrm{thn0}})^2(1+\lambda_1 0.5V_{\mathrm{DD}}) \cong \\ &\cong I_b + \frac{1}{2}\mu_p C_{oxp}\frac{W_3}{L_3}(0.85V_{\mathrm{DD}} - V_{\mathrm{thp0}})^2(1+\lambda_3 0.2V_{\mathrm{DD}}),\end{aligned}, \tag{4}$$

$$V_{tH} \cong V_{\mathrm{thn0}} + \sqrt{\frac{I_b + \frac{1}{2}\mu_p C_{oxp}\frac{W_3}{L_3}(0.85V_{\mathrm{DD}} - V_{\mathrm{thp0}})^2(1+\lambda_3 0.2V_{\mathrm{DD}})}{\frac{1}{2}\mu_n C_{oxn}\frac{W_1}{L_1}(1+\lambda_1 0.5V_{\mathrm{DD}})}}. \tag{5}$$

After V_{in} exceeds the threshold V_{tH}, the following will happen: P_3 turns off, N_1 enters the triode region and P_5 remains active ($I_1 = I_b$). Further, while V_{in} increases to V_{DD}, P_5 enters the triode region and then it turns off.

Decreasing V_{in} from V_{DD} to V_{SS} will determine V_3 to decrease almost linearly, P_5 to go successively in the triode and then in the active regions, and N_1 to enter the triode region; until V_{in} reaches the low threshold V_{tL}, P_3 remains off. When V_{in} equals V_{tL}, the transistor N_1 becomes active ($V_1 \approx 0.4$ V) and the voltage V_2 falls down to V_{SS}; this would result in a large current through P_3 and therefore, N_1 is forced to return quickly back to the triode region. After V_{in} falls below the threshold V_{tL}, P_3 enters the triode region.

The relation $I_1 = I_b$ underlies the low threshold calculation. This time N_1 may operate in the moderate inversion or subthreshold region, depending on the value of I_b, so the EKV model (Enz *et al.*, 1995) should be used instead of (3). For NMOS transistors with $V_{\mathrm{BS}} = 0$ V and $V_{\mathrm{DS}} > 4V_{\mathrm{T}}$, the model takes the form

$$I_{\mathrm{D}} = 2n\mu_n C_{oxn} \frac{W}{L} V_{\mathrm{T}}^2 \ln^2(1 + \exp\frac{V_{\mathrm{GS}} - V_{\mathrm{thn0}}}{2nV_{\mathrm{T}}}),\; n = 1 + \frac{C_{dep}}{C_{oxn}}, \tag{6}$$

where n, C_{dep} and V_{T} are, respectively, the slope factor, the surface depletion capacitance and the thermal voltage. The slope factor n is technology-dependent, taking values in the range [1.1, 1.8], and it decreases slightly with increasing the difference $V_{\mathrm{GS}} - V_{\mathrm{thn0}}$ (also called pinch-off voltage).

The low threshold is given by

$$V_{tL} = V_{\mathrm{thn0}} + 2nV_{\mathrm{T}} \ln\left(\exp\frac{\sqrt{I_b L_1}}{V_{\mathrm{T}}\sqrt{2n\mu_n C_{oxn} W_1}} - 1 \right). \tag{7}$$

By taking the difference between (5) and (7) we obtain the hysteresis value:

$$V_{tH} - V_{tL} \cong \sqrt{\frac{2I_b + \mu_p C_{oxp} \frac{W_3}{L_3}(0.85V_{\mathrm{DD}} - V_{\mathrm{thp0}})^2 (1 + \lambda_3 0.2V_{\mathrm{DD}})}{\mu_n C_{oxn} \frac{W_1}{L_1}(1 + \lambda_1 0.5V_{\mathrm{DD}})}} - \\ - 2nV_{\mathrm{T}} \ln\left(\exp\frac{\sqrt{I_b L_1}}{V_{\mathrm{T}}\sqrt{2n\mu_n C_{oxn} W_1}} - 1 \right). \tag{8}$$

The bias current I_b has a greater influence on the low threshold; the high threshold changes very little. Both switching thresholds and the hysteresis depend on the process variations, supply voltage and temperature.

At high frequencies the following equation should be used instead of (2)

$$I_1 = I_b + I_3 + I_{C1}, \tag{9}$$

where I_{C1} is the discharge current of capacitor C_1; the high threshold V_{tH} will increase. The low threshold V_{tL} should be calculated by using the relation

$$I_1 = I_b - I_{C1}. \tag{10}$$

This time the capacitor C_1 has to be charged by a current derived from the bias current I_b and thus, V_{tL} will decrease.

The capacitor C_2 determines a slight increase of V_{tH} through the current I_3.

3. Simulation Results

Transient responses of the circuit to triangular rail-to-rail input voltages of 50 MHz and 1 GHz are illustrated in Figs. 4 and 5, respectively. The high threshold is almost insensitive to the bias current and increases with frequency. The low threshold is sensitive to both bias current and frequency; in accordance with (7), its dependence on current is not linear. The range of the bias current I_b must be chosen depending on the input frequency.

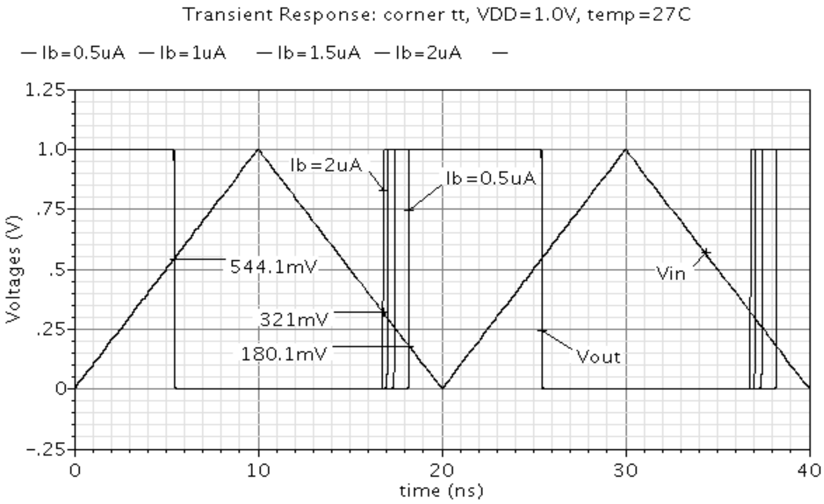

Fig. 4 – Transient responses to 50 MHz input signal.

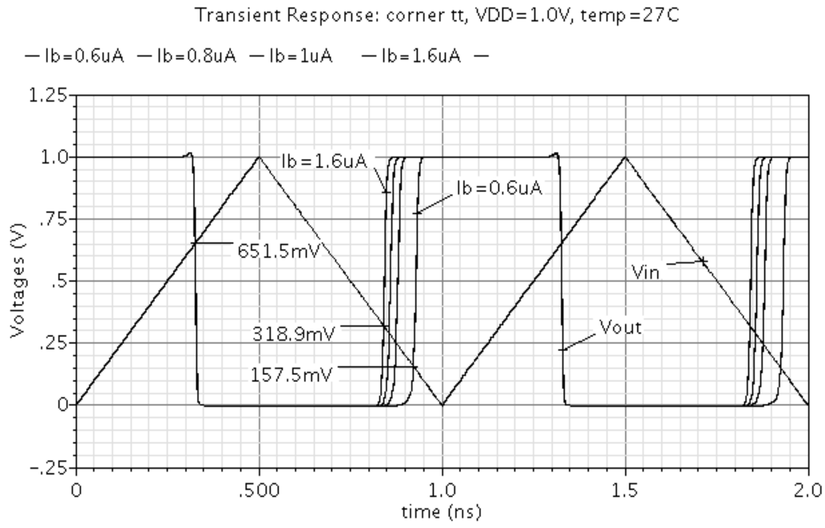

Fig. 5 – Transient responses to 1 GHz input signal.

The influences of the process variations, supply voltage and temperature (PVT) on the two switching thresholds are shown in Figs. 6,…,8; the simulations are performed at 1 GHz input frequency and 2 µA bias current.

The low threshold V_{tL} is more sensitive to the process variations than the high threshold V_{tH}. From ff corner to sf corner, V_{tL} varies (approximately) between 150 mV and 400 mV; V_{tH} varies between 700 mV and 600 mV.

The changes in supply voltage (±100 mV) have a slightly higher influence on the high threshold (about ±50 mV).

Both switching thresholds are weakly dependent on temperature; V_{tL} is slightly more sensitive and it decreases by less than 50 mV with increasing temperature from –40 ºC to 125 ºC.

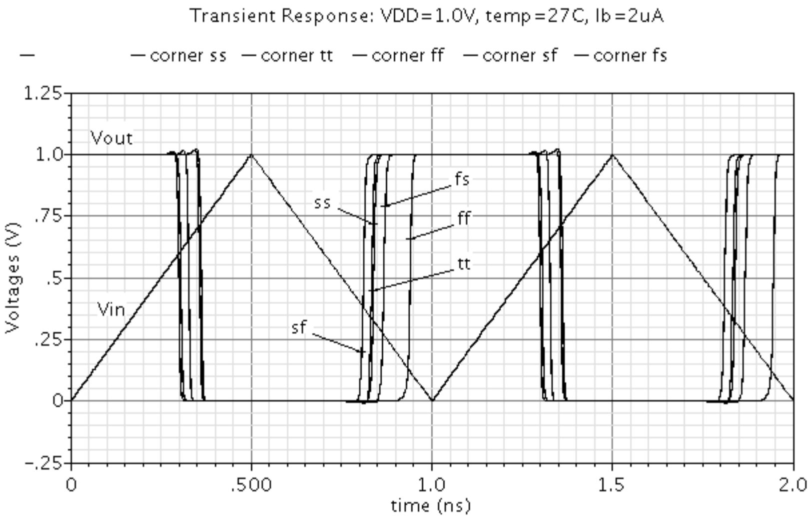

Fig. 6 – Switching thresholds versus process corners.

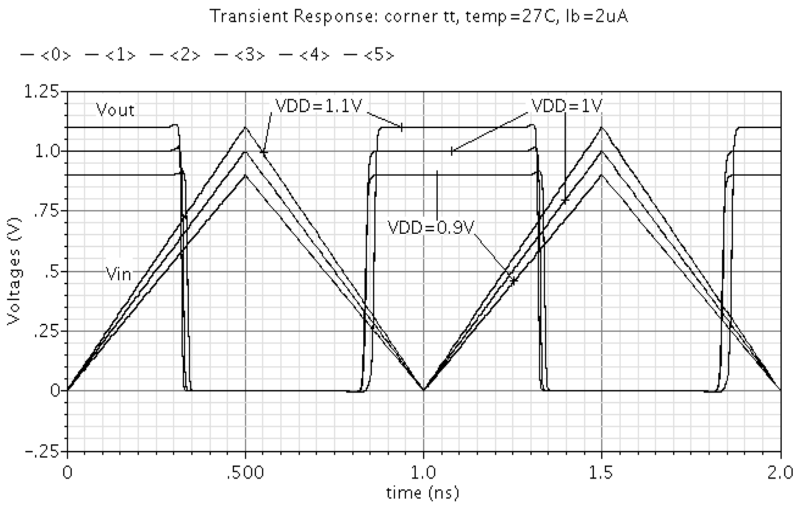

Fig. 7 – Switching thresholds versus supply voltage.

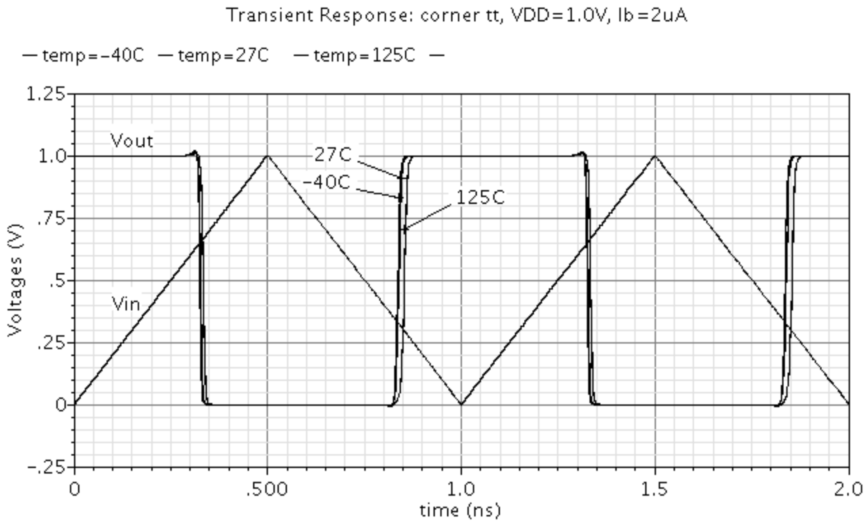

Fig. 8 – Switching thresholds versus temperature.

Fig. 9 shows the rise and fall times of the voltage V_2, at 1 GHz input frequency.

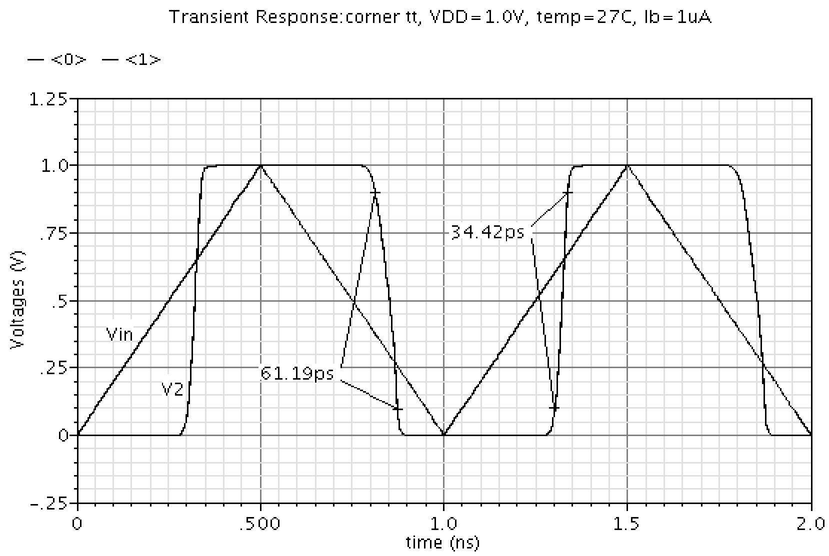

Fig. 9 – Rise and fall times corresponding to voltage V_2.

The current consumption of the circuit at 1 GHz input frequency, in the worst case conditions and 5 µA bias current is depicted in Fig. 10. The root mean square of the supply current is about 50 µA.

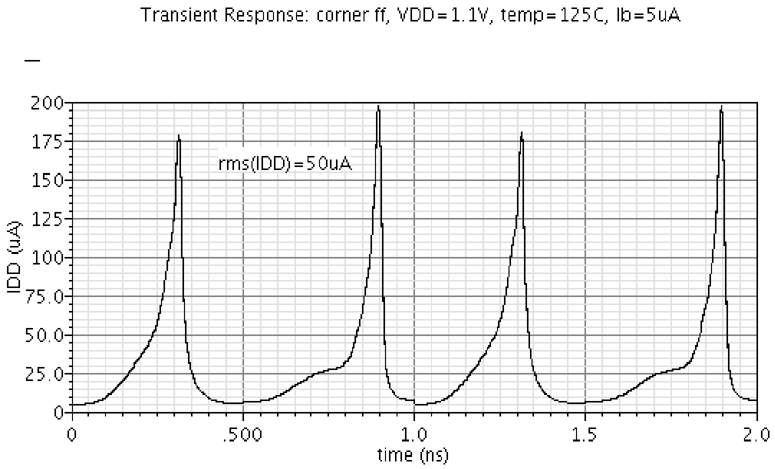

Fig. 10 – Supply current consumption.

The silicon area of the Schmitt trigger in Fig. 2, which includes the load inverter *Inv*, is less than 21 µm^2; the layout is illustrated in Fig. 11. The mirror P_4-P_5 (situated in the upper part) occupies about half of the total area.

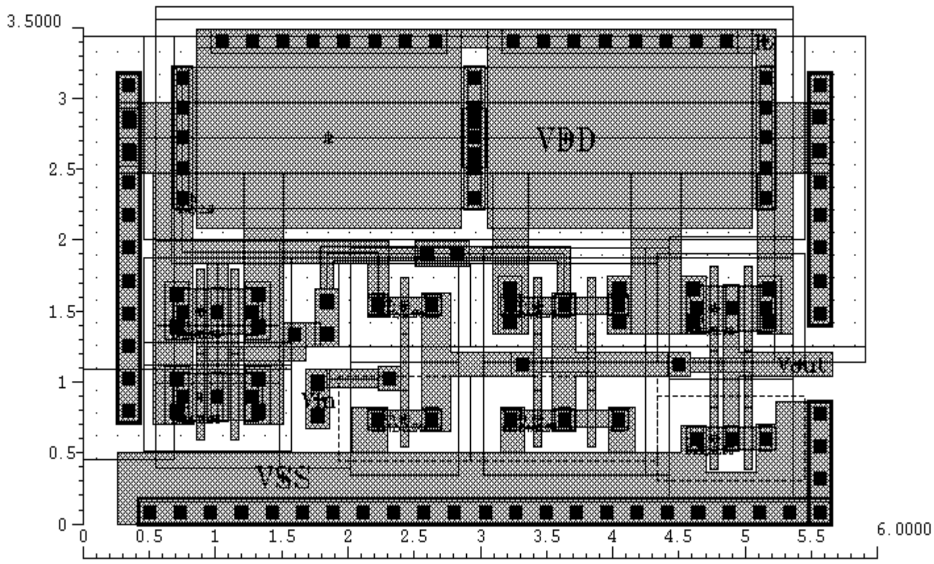

Fig. 11 – Layout view of the proposed Schmitt trigger.

For low-frequency applications the transistors can be sized differently. The channel-length modulation effect can be eliminated by increasing the transistor lengths.

4. Comparisons with Similar Works

The topology of the circuit proposed in this paper is a new one. Comparisons between this work and the ones referenced in this paper are rather difficult to do, because they provide too little information. However, some comparisons with (Yuan 2010) can be done, even if the circuit described there has a differential structure. The comparisons are listed in the Table 1.

Table 1
Comparisons

	This work	Yuan 2010
Process	65 nm CMOS std.	0.18 µm CMOS std.
Supply voltage	[0.9, 1.1] V 1 V nominal	1.8 V nominal
Supply current consumption	50 µA (rms)@1GHz 200 µA (peak)@1GHz	2.61 mA
PVT simulations	shown	not shown
Temperature range	[-40, +125] ºC	not shown
Max. input frequency	5 GHz	not shown
Controlled thresholds (at low frequency)	low threshold $0 < V_{tL} < 0.54$ V	both thresholds $0.95 \text{ V} < V_{tL}, V_{tH} < 1.35$ V
Max. hysteresis (at low frequency)	0.54 V	0.23 V
Rise time Fall time	35 ps@1GHz 61 ps@1GHz	not shown
Silicon area	< 21 µm^2	not shown

5. Conclusions

The new Schmitt trigger described in this work contains only 7 MOS transistors of type 1.0V standard-Vt. The circuit is designed in 65 nm CMOS standard process but can be implemented in any other technology. The silicon area is about 21 µm^2; also, the power consumption is quite small.

The circuit schematic consists of two inverters and two current sources; one of the current sources is controlled by an external bias current that serves to adjust the low switching threshold and also the hysteresis.

Simulations show that both switching thresholds are weakly dependent on temperature. The process variations and supply voltage have greater influences; their compensation up to a certain degree can be made through the external bias current.

The circuit can be used in digital and analog applications up to 5 GHz frequency.

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TRIGGER SCHMITT CMOS CU HISTEREZIS CONTROLAT ÎN CURENT

(Rezumat)

Se prezintă o nouă topologie de trigger Schmitt. Circuitul este proiectat într-o tehnologie CMOS standard de 65 nm şi conține 7 tranzistoare MOS cu tensiuni de prag standard. Tensiunea de alimentare nominală este 1 V, cu toleranța ±10%. Trigger-ul funcționează în gama de temperatură [–40, +125] ºC.

Schema circuitului conține două inversoare; unul este alimentat direct de la sursa de tensiune de 1 V iar celălalt este alimentat prin două surse de current, conectate în paralel. O sursă de current este controlată din exteriorul circuitului cu un current de polarizare de ordinul µA; prin intermediul acestuia se reglează pragul de comutare inferior şi implicit histerezisul.

Pragurile de comutare sunt puțin dependente de temperatură; influențe mai mari asupra lor au variațiile procesului tehnologic şi ale tensiunii de alimentare.

Circuitul ocupă o arie de siliciu de aproximativ 21 µm^2, are un consum de current relativ mic şi poate fi utilizat în diverse aplicații (analogice şi digitale). Tensiunea de intrare a circuitului poate să aibă frecvențe până la 5 GHz.