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# LOW OFFSET, HIGH RESOLUTION DIFFERENTIAL CURRENT COMPARATOR FOR LOW FREQUENCY APPLICATIONS

BY

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**Abstract.** A new topology of differential current comparator with perfectly symmetrical structure is presented. The proposed circuit is designed in 65 nm CMOS standard process and operates in the temperature range [–30, +130] °C. Implementation can be done either by using core devices ($V_{DD}$ = 1.0 V) or I/O devices ($V_{DD}$ = 2.5 V). The comparator is very insensitive to temperature, supply voltage and process corners, and has high resolution. It can detect differences the order of magnitude 10 pA of between the input currents. The input offset, due to device parameter mismatches, is about 9 nA at 1 µA reference current and it can actually be considered the accuracy of the proposed current comparator.

**Key words:** current comparator; PVT sensitivities; input offset; resolution.

## 1. Introduction

A current comparator is a circuit that compares two input currents and indicates the result as a voltage with logic levels High or Low.

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Several topologies of current comparators have been proposed. Some comparators include a difference stage. The one shown in Fig.1 *a* is used in (Chavoshisani *et al.*, 2011; Sridhar *et al.*, 2015); this circuit is not symmetrical, relative to the inputs $I_1$, $I_2$ and the output $I_{diff}$.

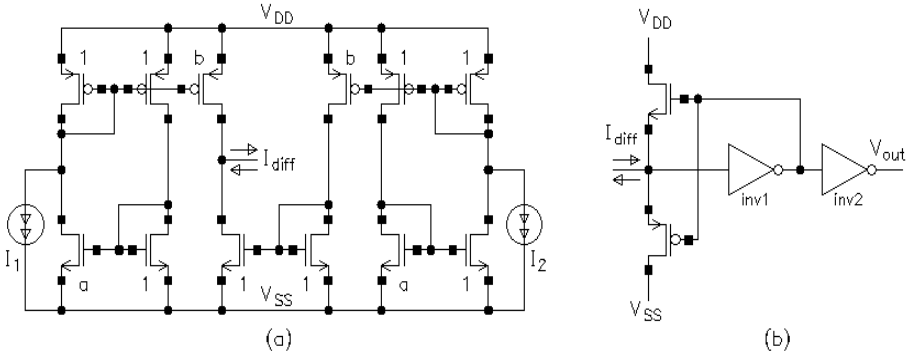



Fig. 1 – *a* – Current difference stage; *b* – Current switch comparator.

The difference between $I_1$ and $I_2$ in Fig. 1 *a* is carried out *via* current mirrors and is given by

$$I_{diff} \simeq \frac{b}{1-a}(I_1 - I_2), \tag{1}$$

where $a < 1$ and $b \geq 1$ are two constants. The accuracy of this operation is affected by supply voltage variations and device mismatches.

Converting $I_{diff}$ into a rail-to-rail voltage may be achieved by means of the current switch comparator depicted in Fig. 1 *b* and proposed by Traff (1992). Improvements of this circuit are presented by Tang *et al.* (2009) and Sridhar *et al.* (2015); more inverters are inserted in order to reduce the dead-band region of the source follower input stage.

Another way to convert $I_{diff}$ into a rail-to-rail voltage is shown in Fig. 2 (Chasta, 2012). The circuit contains a latch structure and may produce hysteresis in the output voltage.

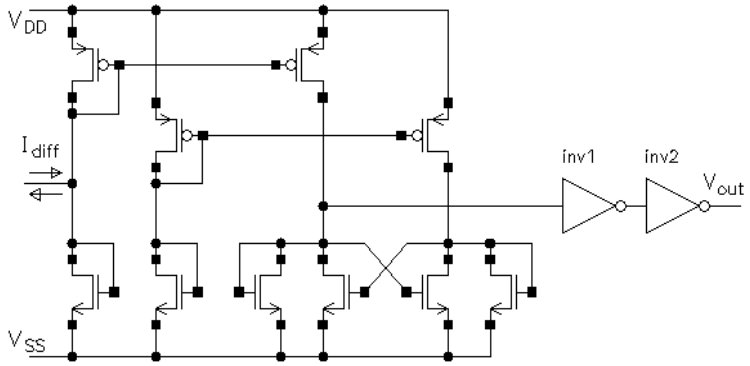



Fig. 2 – Current comparator with hysteresis.

The comparison of two currents can be done without using a current difference stage, as shown in Fig. 3 (Lin *et al.*, 2010). The voltages $v_1$ and $v_2$ produced by the input currents are then amplified and compared, using several simple stages (not illustrated in the figure), in order to get the output logic voltage.

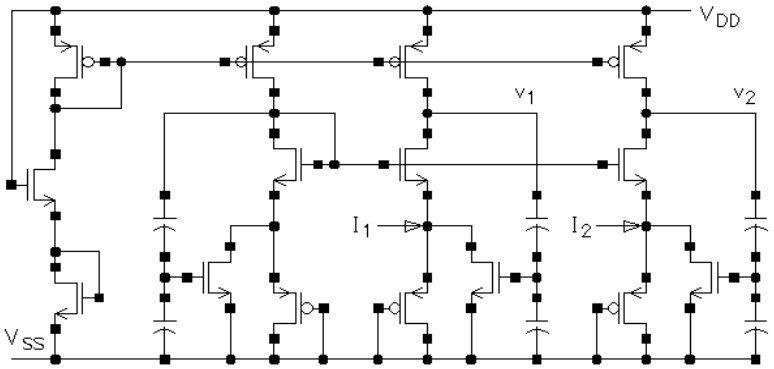



Fig. 3 – Current comparator without difference input stage.

In the next section we present a new current comparator which does not perform the difference operation between the input currents.

## 2. Description of the Proposed Circuit

The schematic of the proposed current comparator, shown in Fig. 4, is based on a latch structure. The current $I_{in}$ is compared with the reference current $I_{ref}$ and two output logic voltages are produced, $V_{out1}$ and $V_{out2}$.

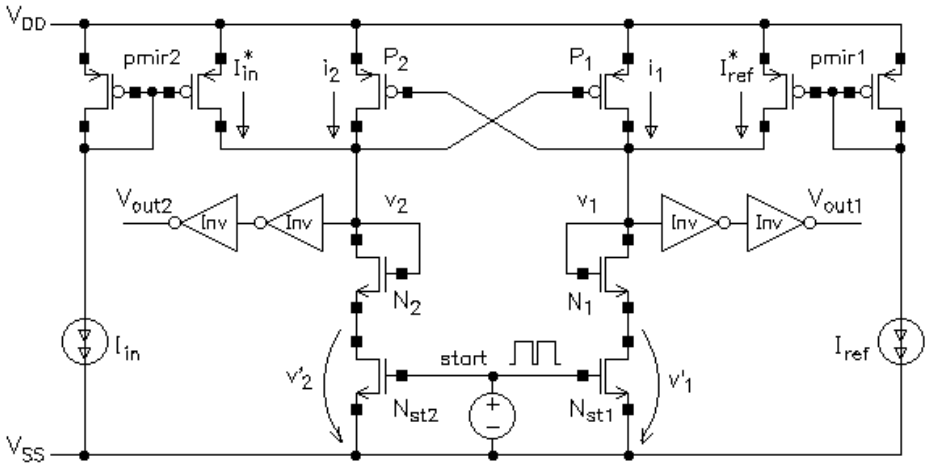



Fig. 4 – The proposed differential current comparator.

The circuit needs a control voltage (*start*) which acts as a reset signal (active Low). The schematic is perfectly symmetrical in relation to inputs and outputs. The two current mirrors named "pmir1" and "pmir2" are identical. Also, the transistors of the pairs $P_1$-$P_2$, $N_1$-$N_2$ and $N_{st1}$-$N_{st2}$ have the same sizes.

All transistors have relatively large sizes, except those in the inverters called "Inv", in order to minimize the influence of device mismatches on the accuracy of comparison. As expected, this implies a lower operating speed.

We may adjust the transistor sizes and the multiplying factor of current mirrors so that we get the best resolution for a particular $I_{ref}$ value.

By using appropriate transistor models, the circuit in Fig. 4 can be implemented to operate with nominal supply voltage of 1.0 V or 2.5 V, as required. Moreover, it has a complementary version (Fig. 5).

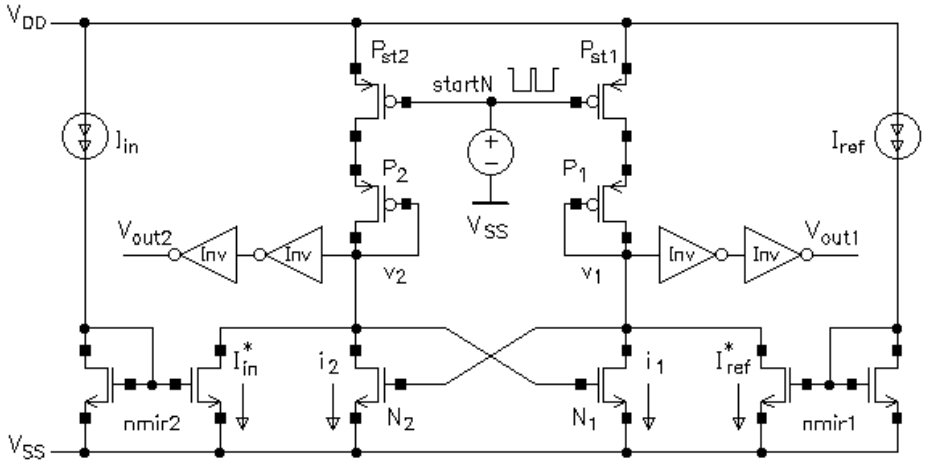



Fig. 5 – Complementary version of the circuit in Fig. 4.

To explain the comparator operation we use the signals presented in Fig. 6, these are captured from a transient simulation of the circuit in Fig. 4 with 2.5 V supply voltage. The current mirrors multiply by 2 the input currents $I_{in}$ and $I_{ref}$.

When "start" is Low ($V_{SS}$), both transistors $N_{st1}$, $N_{st2}$ are off and the voltages $v_1$, $v_2$, $V_{out1}$, $V_{out2}$ reach the maximum value $V_{DD}$; the previous comparison result is deleted or canceled. The output transistors of pmir1, pmir2 operate in triode region at zero current and $P_1$, $P_2$ are off.

When the "start" signal goes toward $V_{DD}$ (High), $N_{st1}$ and $N_{st2}$ pass the active region, and then enter the triode region. During this transition, the output capacitance of pmir1 and pmir2 increases. This is the cause for the overshoots occurring in $I_{ref}^*$ and $I_{in}^*$ right after the "start" switching. Then $I_{ref}^*$ and $I_{in}^*$ tend to $2I_{ref}$ and $2I_{in}$, respectively, while $v_1$ and $v_2$ are decreasing. Transistors $P_1$, $P_2$ enter the conduction region and at one moment they trigger the positive reaction.

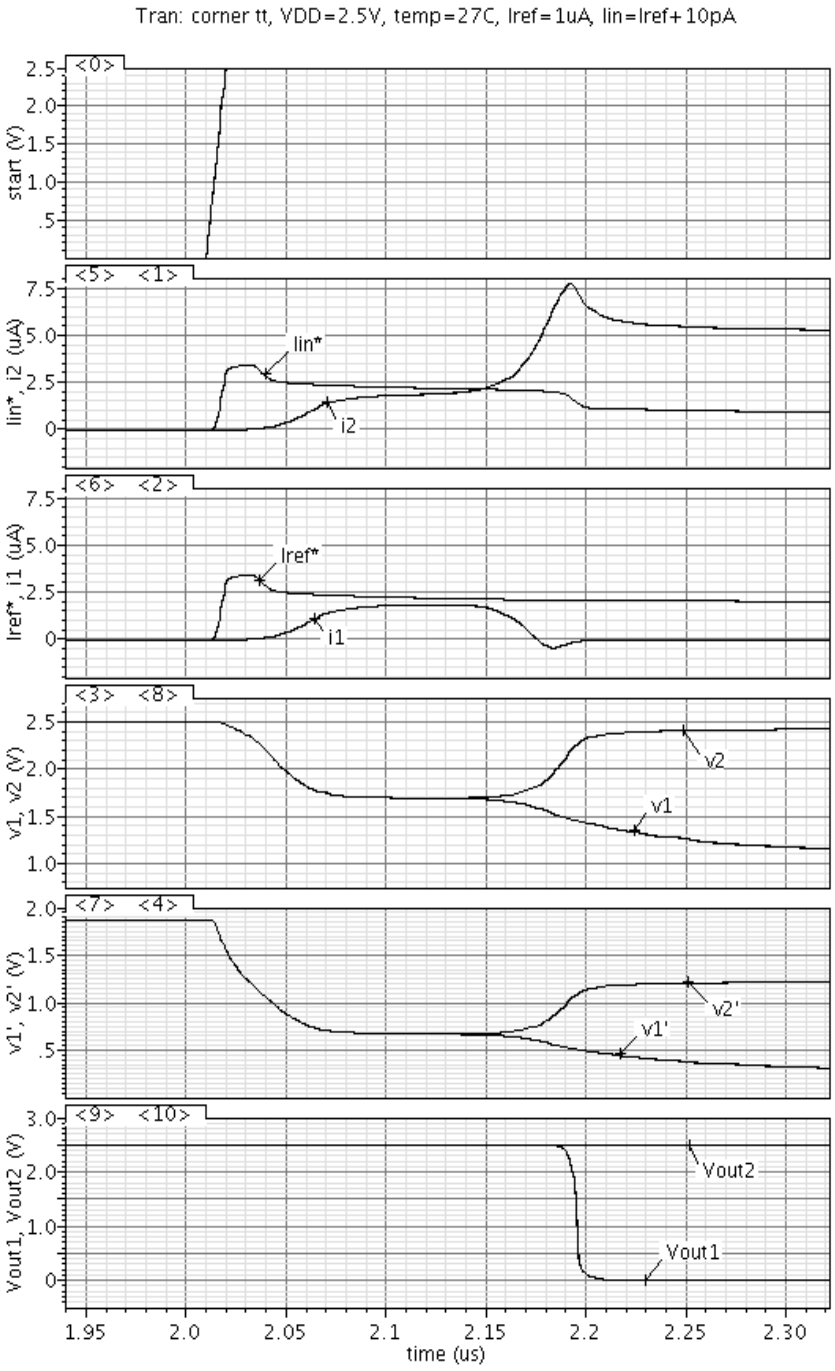



Fig. 6 – Transient responses of the circuit in Fig. 4.

If the difference between the input currents is large enough, then this will dictate the final state of the circuit. Otherwise, the asymmetries caused by device mismatches will lead to an unpredictable state.

In the simulation that produced the results in Fig.6 it has been assumed that $I_{in}$ is greater than $I_{ref}$. Also, mismatches were not taken into account. In these circumstances, a difference of only 10 pA between the input currents is enough to force the final state $V_{out1}$ = Low, $V_{out2}$ = High. In this state $P_1$ is off, the output transistor of pmir2, $P_2$ and $N_{st1}$ operate in the triode region; the output transistor of pmir1 and $N_{st2}$ operate in the active region. It is mandatory for $v_1$ to decrease below the transition voltage of the inverter connected to $v_1$. The value reached by $v_1$ is given by:

$$v_1 = V_{GS,N1} + v'_1 \simeq V_{th,N1} + 2\sqrt{\frac{I_{ref}}{\mu_n C_{ox}}\left(\frac{L}{W}\right)_{N1}} + \frac{I_{ref}}{\mu_n C_{ox}(V_{DD} - V_{th,Nst1})}\left(\frac{L}{W}\right)_{Nst1}, \quad (2)$$

where: $\mu_n$, $C_{ox}$, $W/L$ and $V_{th}$ are the mobility of electrons, the oxide capacitance per unit area, the channel sizes and the threshold voltage.

If $I_{in}$ is less than $I_{ref}$, then the circuit goes into the state $V_{out1}$ = High, $V_{out2}$ = Low which is complementary to $V_{out1}$ = Low, $V_{out2}$ = High.

The difference between the input currents has relatively little influence on the response time of the comparator (about 180 ns); it is mainly determined by the sizes of transistors.

## 3. Simulation Results

Transient responses of the proposed current comparator, in the absence of device mismatches, are illustrated in Figs. 7 and 8.

Variations of supply voltage, temperature and process corners are considered in Fig. 7. In all cases the two input currents are $I_{ref}$ = 1µA and $I_{in}$ = $I_{ref}$ ± 50 pA. The latter changes its value alternatively, every 5 µs, that means a frequency of 100 kHz. The comparison is done 4 times faster, at every 2.5 µs, which means that the control signal "start" has 400 kHz frequency. This value is close to the upper speed limit at which the comparisons still produce accurate results. Charts for both output voltages $V_{out1}$ and $V_{out2}$ are provided only for supply voltage variations; $V_{out2}$ diagrams are no longer illustrated for temperature and process variations.

The range of the reference current $I_{ref}$ and the current consumption of the circuit at 400 kHz sampling frequency are shown in Fig. 8. The current comparator operates properly for a reference current belonging to the range [0.6, 1.6] µA. For other values of $I_{ref}$, some transistors in the circuit schematic should be resized according to (2). The supply current $I_{DD}$ depends mainly on operating frequency and $I_{ref}$. Most of the consumption is due to the four inverters, especially those connected to voltages $v_1$ and $v_2$, because the levels of

$v_1$ and $v_2$ are close to the transition voltage for a relatively long time. The supply voltage and process corners have less influence on the supply current consumption. The root mean square of $I_{DD}$, corresponding to $I_{ref}$ = 1.6 µA (curve 3 in Fig.8 ), is about 93 µA.

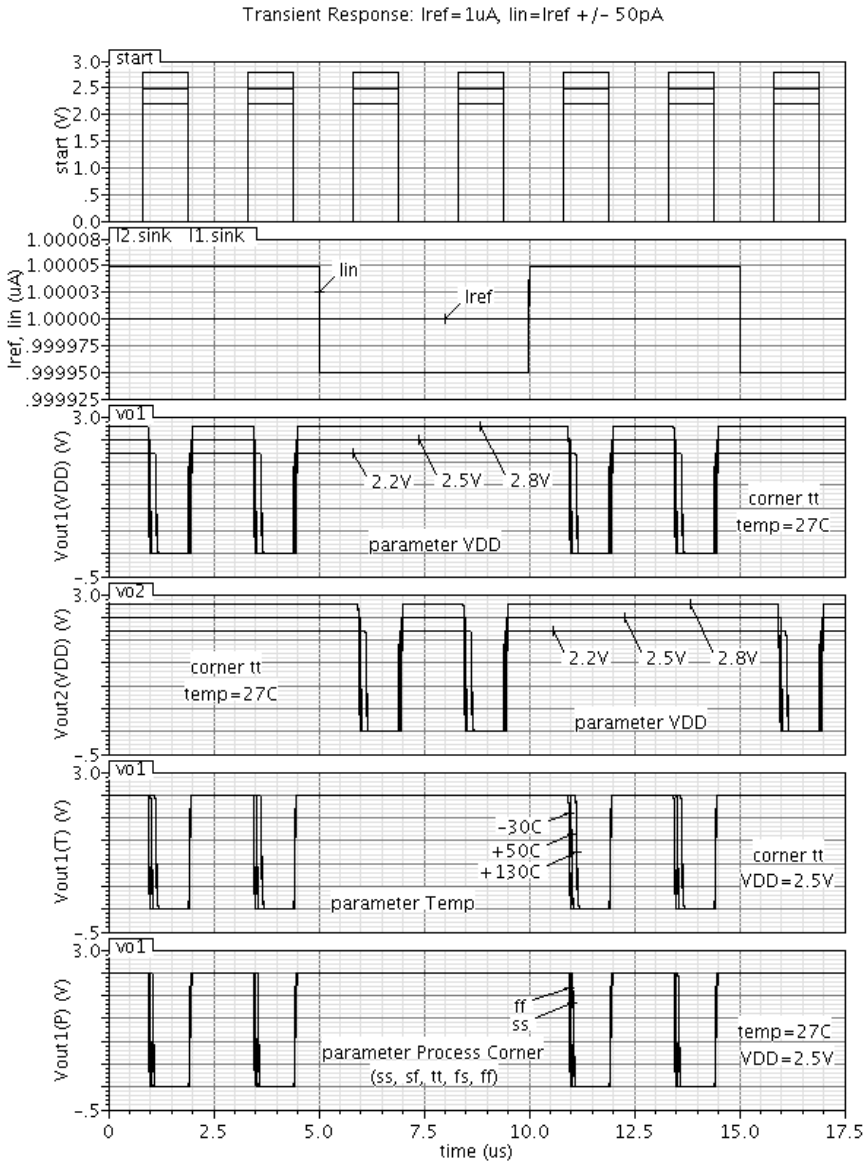



Fig. 7 – Influences of supply voltage, temperature and process corners on the current comparator responses.

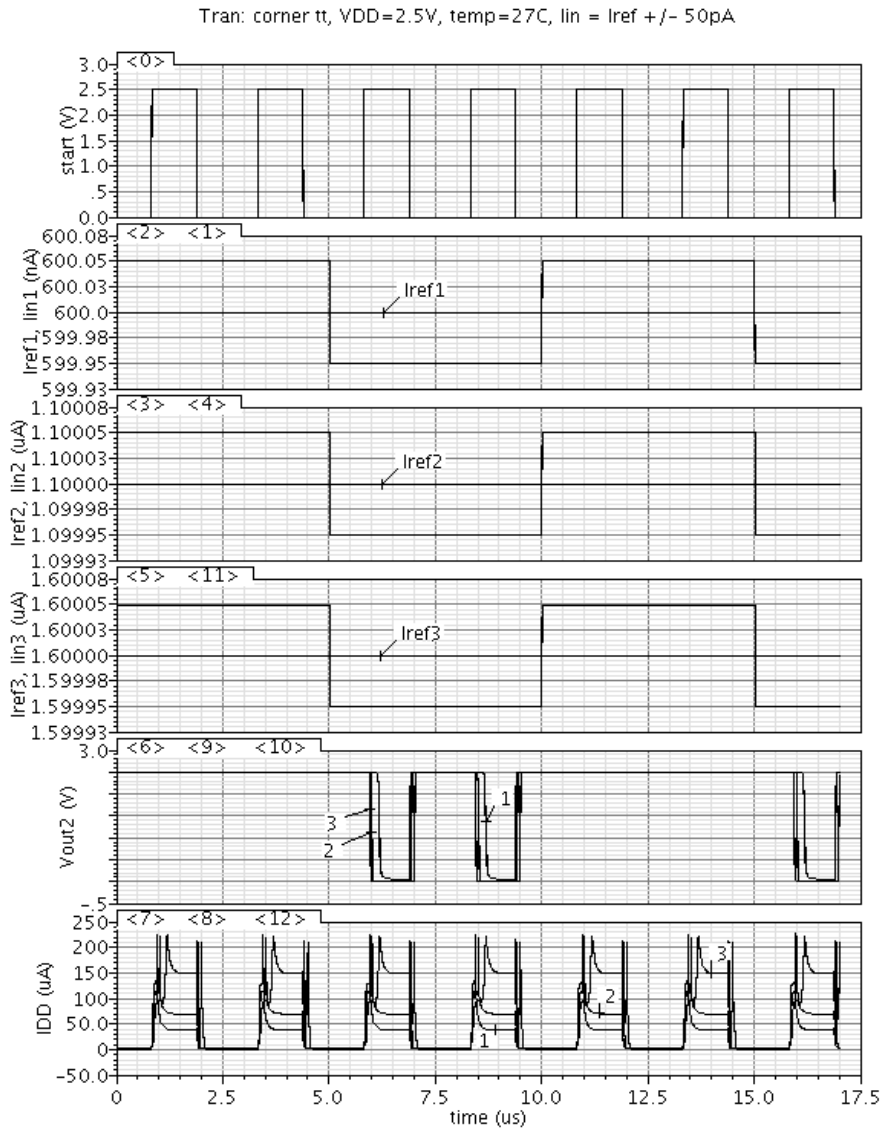
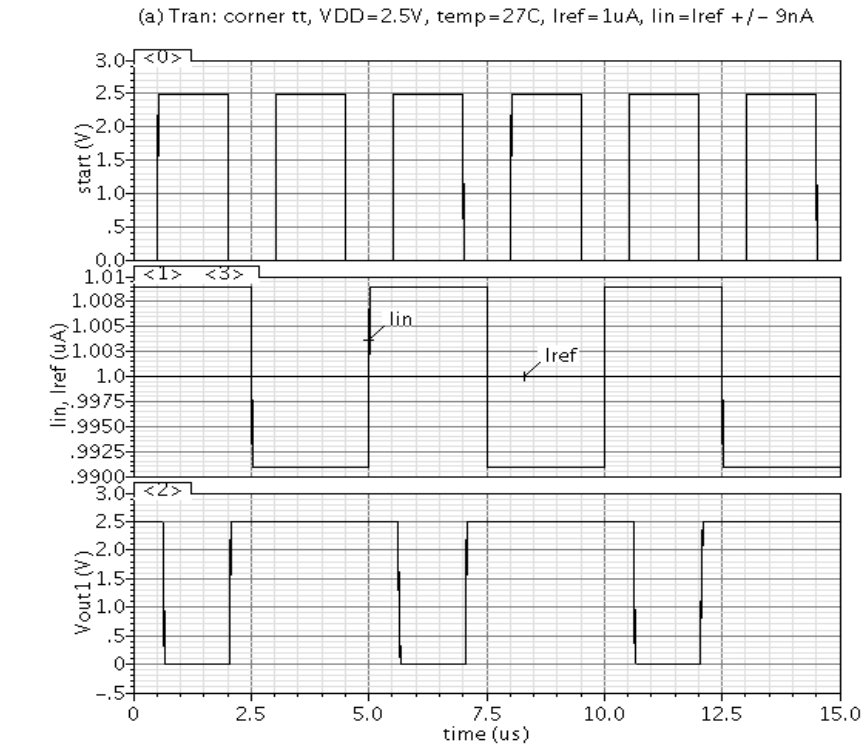
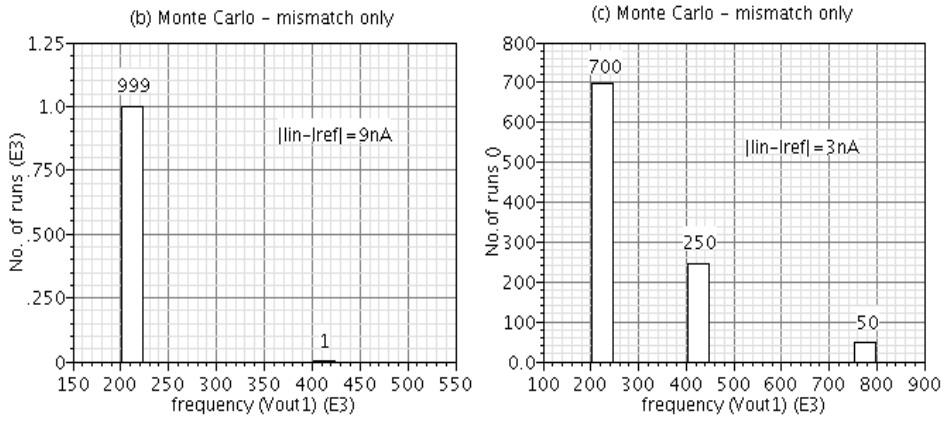



Fig. 8 – Reference current range and supply current consumption.

The effects of mismatches on the comparator responses are determined via Monte Carlo simulations. The signals in Fig. 9 *a* show the signals applied to the comparator inputs and the expected result. The "start" signal forces one comparison every 2.5 µs, so the expected result ($V_{out1}$) should have a frequency of 200 kHz. Because of the device parameter mismatches, some responses may be wrong and therefore the output frequency will change.




*a*




*b* *c*

Fig. 9 – Monte Carlo simulation: (*a*) input signals and the expected result; (*b*, *c*) results.

The simulation results shown in Fig. 9 *b* indicate that 999 responses out of 1,000 are correct. This means that the difference $|I_{in} - I_{ref}|$ of 9 nA is very close to the input offset and represents the circuit accuracy. If $|I_{in} - I_{ref}|$ is reduced to 3 nA, then we get the results in Fig. 9 *c*; in this case 300 responses

are wrong. It should be noted that some correlations between devices were considered; this implies good matching in layout for transistors in the pairs $P_1$-$P_2$, $N_1$-$N_2$, $N_{st1}$-$N_{st2}$ and, respectively, for those in "pmir1" and "pmir2".

The layout of the proposed circuit occupies 24 µm × 29 µm of silicon area and is shown in Fig. 10. It has perfect symmetry on the horizontal axis.

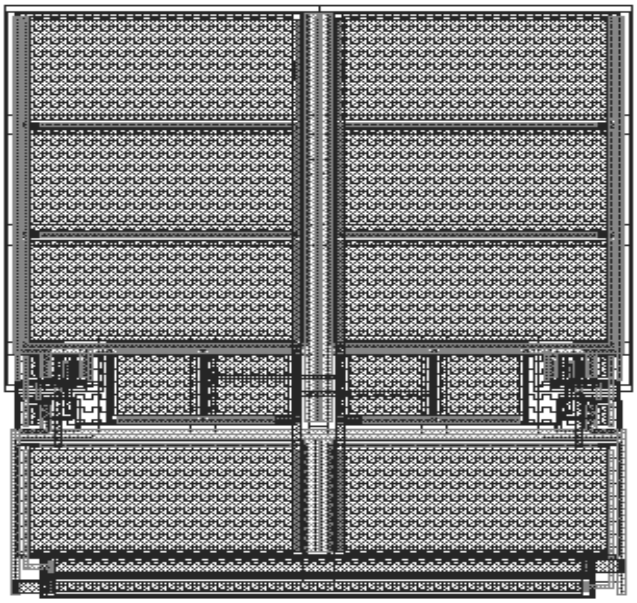


Fig. 10 – Layout view of the proposed differential current comparator.

## 4. Comparisons with Similar Works

Comparisons between this work and those ones cited here are listed in Table 1. Note that the current comparator presented in (Tang *et al*., 2009) is not complete; input is taken as the difference between input currents, so the actual speed of the circuit may be lower than indicated in the table.

The main parameters of a differential current comparator are the resolution, input offset and speed.

As indicated by the title of this work, the proposed comparator has low speed and operates properly up to 400 kHz. Increasing the frequency at 1 MHz is possible by decreasing the sizes of some transistors, but this implies the increase of the offset.

Simulation results related to the offset are not covered in any of the works cited. Also, the influence of variations in temperature, supply voltage and process are not given, except for (Sridhar *et al*., 2015), where the impact of process on the delay and power dissipation is analyzed.

**Table 1**
*Comparisons*

| | This work | Tang *et al*., 2009 | Lin *et al*., 2010 | Chavoshisani *et al.*, 2011 | Chasta 2012 | Sridhar *et al*., 2015 |
|---|---|---|---|---|---|---|
| Process | 65 nm CMOS std. | 0.18 µm CMOS std. | 0.35 µm CMOS std. | 0.18 µm CMOS std. | 0.18 µm CMOS std. | 0.18 µm CMOS std. |
| Supply voltage | 2.5 V 1.0 V | 1.8 V 1.2 V | 3.0 V | 1.8 V | 3.0 V | 1.8 V |
| Input range | µA | – | – | tens of µA | – | µA |
| $\Delta I_{in}$ $I_{in}$ - $I_{ref}$ | ± 10 pA | ± 100 nA | ± 100 nA | ± 1 µA | ± 1 µA | ± 5 nA |
| Input offset | 9 nA | – | – | – | – | – |
| Speed | 400 kHz | 10 MHz | 25 MHz | 100 MHz | – | 5 MHz |
| Silicon area | 24×29 $\mu m^2$ | – | 72×60 $\mu m^2$ | – | – | – |
| Power cons. | 230 µW | – | 1.16 mW | 300 µW | 2.3 mW | 646 µW |

## 5. Conclusions

A differential current comparator with symmetrical structure, which can be designed to operate either with 2.5 V or 1.0 V supply voltage, is described. It also has two complementary versions. The simulation results demonstrate good characteristics of the circuit, namely 10 pA resolution, 9 nA input offset and very low sensitivities to temperature, supply voltage and process corners.

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## COMPARATOR DIFERENȚIAL DE CURENT CU OFFSET MIC ŞI REZOLUȚIE MARE, PENTRU APLICAȚII DE JOASĂ FRECVENȚĂ

(Rezumat)

Se prezintă un comparator diferențial de curent cu structură simetrică, în două versiuni complementare. Circuitul este proiectat într-o tehnologie CMOS standard de 65 nm, conține numai tranzistoare şi poate să funcționeze fie cu tensiunea de alimentare nominală de 2.5 V fie de 1.0 V, în gama de temperatură [–30, +130] ºC.

Circuitul compară un curent de referință de ordinul μA cu un alt current constant sau variabil în timp, de joasă frecvență (sute de kHz). Comparatorul are capacitate de memorare a rezultatului iar operația este controlată de un semnal (tensiune logică) cu rol de reset. Funcționarea nu este sensibilă la variațiile temperaturii, tensiunii de alimentare şi procesului tehnologic.

Caracteristicile principale ale circuitului propus sunt: rezoluție 10 pA, offset la intrare 9 nA, consum de putere şi arie de siliciu relativ mici.