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LINEAR CURRENT-TO-FREQUENCY CONVERTER WITH WIDE OUTPUT RANGE

BY

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Abstract. A linear CMOS circuit that converts an input current in the range [0.1, 100] µA into an output frequency in the range [0.1, 100] MHz is presented. The circuit is designed in 65 nm CMOS standard technology and operates in the temperature range [-25, +125] °C with supply voltage from 0.9 V to 1.1 V. The relative linearity error is less than 1.42%. The output frequency depends on process variations, supply voltage and temperature (PVT) but it keeps strong linearity with the input current. The circuit dissipates 232 µW in the worst operating conditions.

Key words: current-to-frequency converter; linear circuit; linearity error; PVT sensitivities.

1. Introduction

Linear current-to-frequency converters have transfer characteristics that pass through the origin. This property makes the distinction between circuits of this type and current-controlled oscillators with linear tuning. In both cases, the

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constant of proportionality between the input current and output frequency is called conversion-gain.

Circuit topologies similar to or derived from that shown in Fig. 1 are often used in designing of relaxation oscillators (Imbrea, 2014), voltage (current)-controlled oscillators, voltage-to-frequency converters (Azcona *et al.*, 2011; Valero *et al.*, 2011; Wang *et al.*, 2006) and current-to-frequency converters (Yadav *et al.*, 2013).

A voltage-to-frequency converter may contain a voltage-to-current converter followed by a current-to-frequency converter.

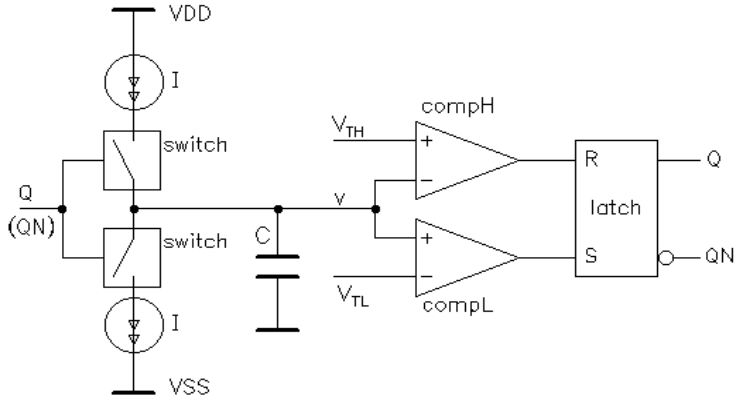

Fig. 1 – Generic current-to-frequency conversion principle.

The current I, used to charge and discharge the capacitor C, and the threshold voltages V_{TH}, V_{TL} of the window comparator may come from current and voltage reference circuits, respectively. Also, the capacitor C may be of MIM type (metal-insulator-metal). All these design considerations aim to achieve high performance circuits, less sensitive to PVT variations.

The equation underlying the circuit in Fig. 1 is:

$$f_{Q(QN)} = \frac{I}{2C(V_{TH} - V_{TL})}, \tag{1}$$

where $f_{Q(QN)}$ represents the frequency of the digital outputs Q and QN. Inherently, the output frequency $f_{Q(QN)}$ is affected to a certain degree by the circuit nonlinearities and PVT variations.

The current-to-frequency converter proposed here may also be considered as derived from that one depicted in Fig. 1. The window comparator made up by the two voltage comparators “compL” and “compH” is no longer used. There are two capacitors instead of one; these are alternatively charged by the input current up to a switching threshold determined by the latch and then are discharged suddenly. Despite the fact that the switching threshold is not very accurate, the conversion is done with quite small linearity errors.

2. Circuit Description

The schematic of the proposed current-to-frequency converter is shown in Fig. 2. The input current is termed I_{in}. There are two complementary output voltages, v_{o1} and v_{o2}.

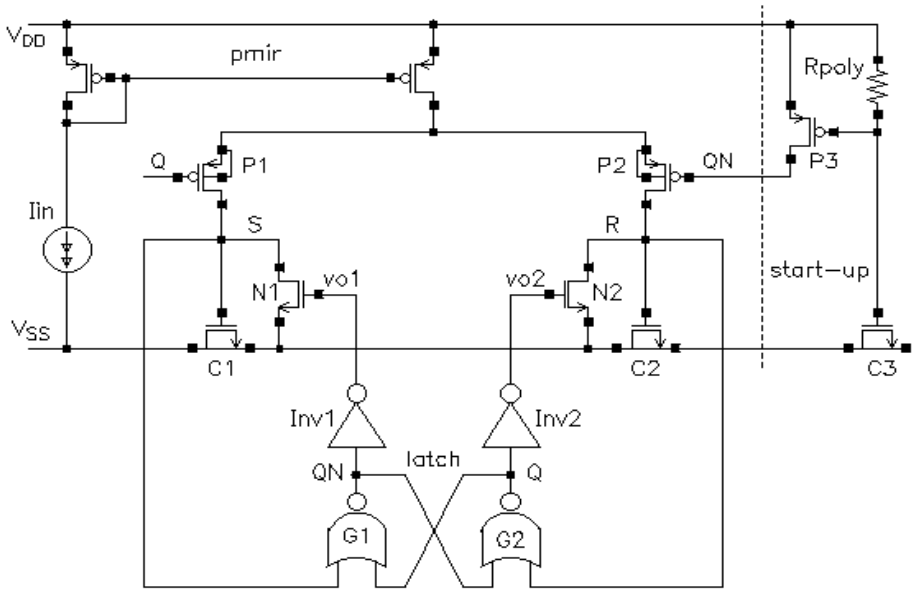

Fig. 2 – Schematic of the proposed current-to-frequency converter.

Transistors N_1, N_2, P_1, P_2, P_3 and those inside inverters Inv1, Inv2 and NOR2 gates G1 and G2 are core devices with standard V_{th} (threshold voltage). These four logic gates are custom cells, not standard library cells. Capacitors C_1, C_2 and C_3 are 2.5 V NMOS native transistors; C_1 and C_2 have identical size. The two PMOS transistors making up the current mirror "pmir" are 2.5 V standard devices. As shown in Fig. 2, a start-up circuitry is needed; the polysilicon resistor R_{poly} and capacitor C_3 occupy small silicon area, having relatively small values (tens of kΩ and tens of fF, respectively).

The time diagrams in Fig. 3, captured from a transient simulation in nominal operating conditions, help explain the circuit operation.

Most of the time both control inputs of the latch, S (Set) and R (Reset), are inactive and the latch keeps its state unchanged: Q = Low (QN = High) or Q = High (QN = Low). Except for small delays, the outputs v_{o1} and v_{o2} are identical with Q and QN, respectively.

During the state Q = Low the capacitor C_2 is short-circuited by N_2 and the voltage across C_1 (*i.e.*, Set) increases approximately linearly, starting from 0 V, as described by (2). When it reaches a certain threshold $V_{t\,NOR}$, determined by

G1, the signal S becomes active and the latch switches to state Q = High.

$$v_{C_1}(t) \simeq \frac{I_{in}}{C_1} t. \tag{2}$$

During the state Q = High the capacitor C_1 is short-circuited by N_1 and the voltage across C_2 (*i.e.*, Reset) increases approximately linearly. Considering that charging of C_1 and C_2 takes T_1 and T_2 time intervals and gates G_1, G_2 have the same switching threshold, the period and frequency of oscillation are:

$$T_{vo1(vo2)} = T_1 + T_2 \simeq \frac{V_{t\,NOR}}{I_{in}}(C_1 + C_2), \;\; f_{vo1(vo2)} \simeq \frac{I_{in}}{(C_1 + C_2)V_{t\,NOR}}. \tag{3}$$

Eqs. (1) and (3) have slightly different forms but they are equivalent.

The threshold voltage $V_{t\,NOR}$ can be adjusted between certain limits by suitably sizing of NMOS and PMOS transistors inside NOR2 gates.

From Fig. 3 we can see that Set and Reset start increasing with a slope greater than that given by eq. (2). This is due to higher source-drain voltage across "pmir" output transistor when charging of C_1 or C_2 begins.

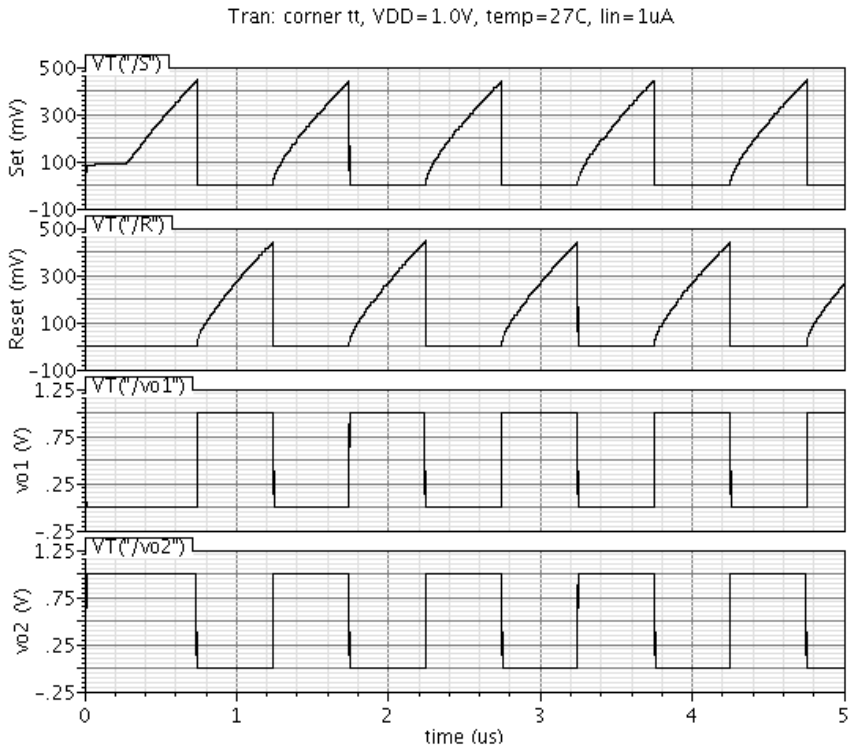

Fig. 3 – Transient responses of the circuit in Fig. 2.

3. Simulation Results

The transfer characteristic of the proposed current-to-frequency converter and the conversion errors are shown in Fig. 4. The absolute and relative linearity errors are calculated using (4), where f_{ideal} is the frequency of an ideal response. The conversion-gain of the circuit is 1 MHz/µA.

$$\begin{cases} \text{Abs.error} = f_{vo1} - f_{\text{ideal}}, \\ \text{Rel.error} = \dfrac{f_{vo1} - f_{\text{ideal}}}{f_{\text{ideal}}}. \end{cases} \tag{4}$$

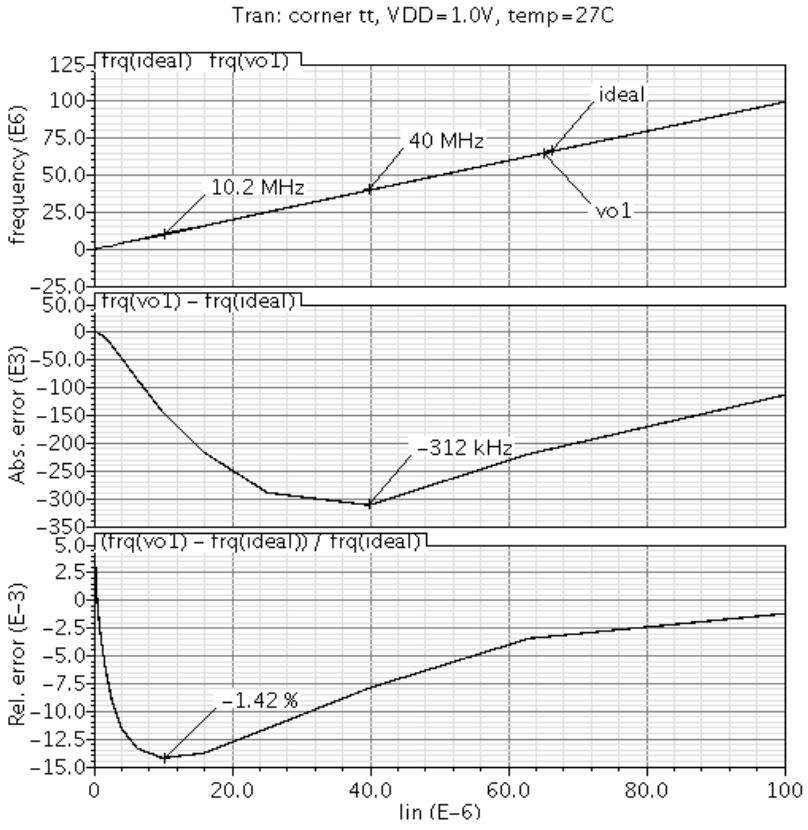

Fig. 4 – Transfer characteristic and linearity errors.

The maximum absolute error is about – 312 kHz at 40 µA input current, which means 39.688 MHz output frequency instead of 40 MHz. The maximum relative error is – 1.42% at 10.2 µA input current.

A slight increase of the input current range is possible. Below 100 nA, the errors get bigger mainly due to leakage. Above 100 µA, we must enlarge some transistors.

The influences of PVT variations on the transfer characteristic are illustrated in Figs. 5,...,7.

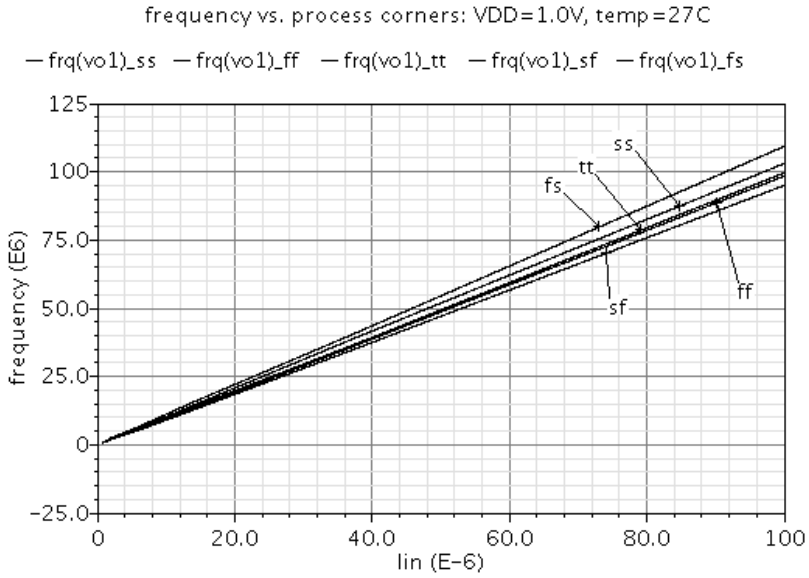

Fig. 5 – Influence of process corners on transfer characteristic.

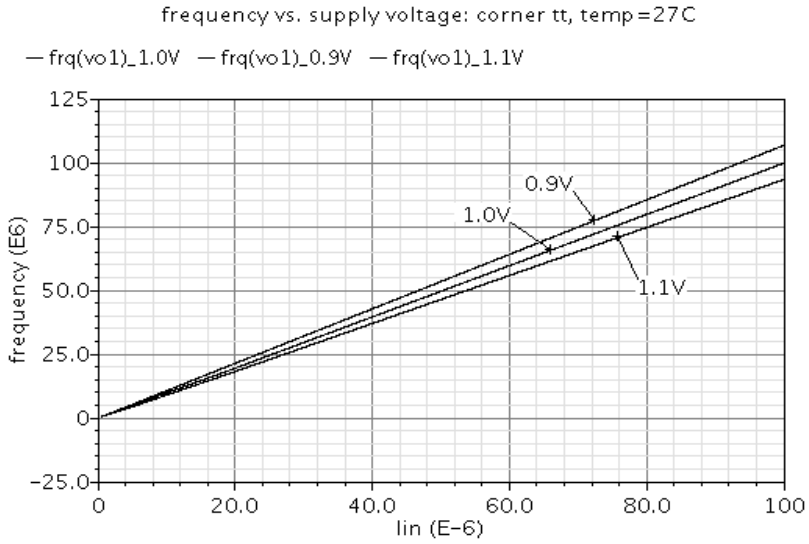

Fig. 6 – Influence of supply voltage on transfer characteristic.

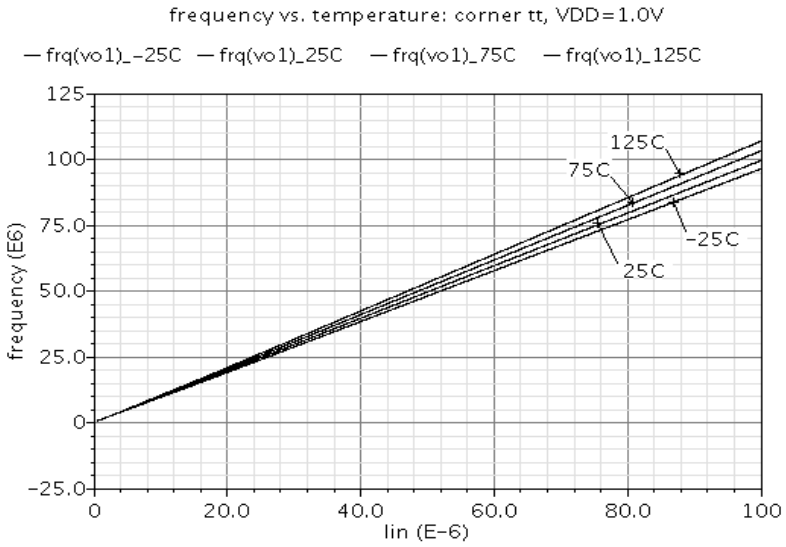

Fig. 7 – Influence of temperature on transfer characteristic.

From the three figures above we may notice that in all cases the circuit keeps the linear transfer characteristic; only its slope is changing because of PVT variations. The influence of process corners, supply voltage and temperature are comparable. The conversion-gain changes from 0.94 MHz/µA to 1.1 MHz/µA.

PVT influences, presented separately in previous figures, may diminish each other or they can cumulate. The extreme cumulating cases are shown in Fig. 8.

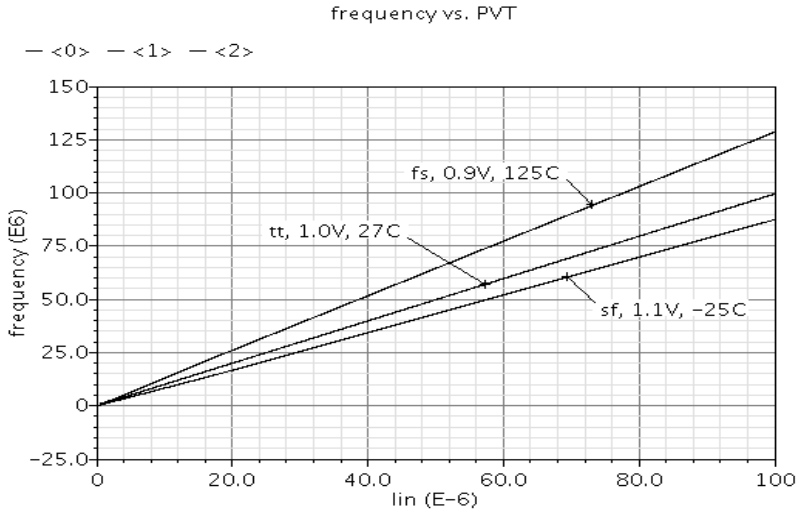

Fig. 8 – Influence of temperature on transfer characteristic.

The conversion-gain decreases to 0.87 MHz/µA in the slow-fast corner, at –25 ºC and 1.1 V supply voltage; it increases to 1.28 MHz/µA in the fast-slow corner, at 125ºC and 0.9 V supply voltage.

The highest current consumption of the proposed converter is shown in Fig. 9. In these operating conditions (worst case) the power consumption is about 232 µW.

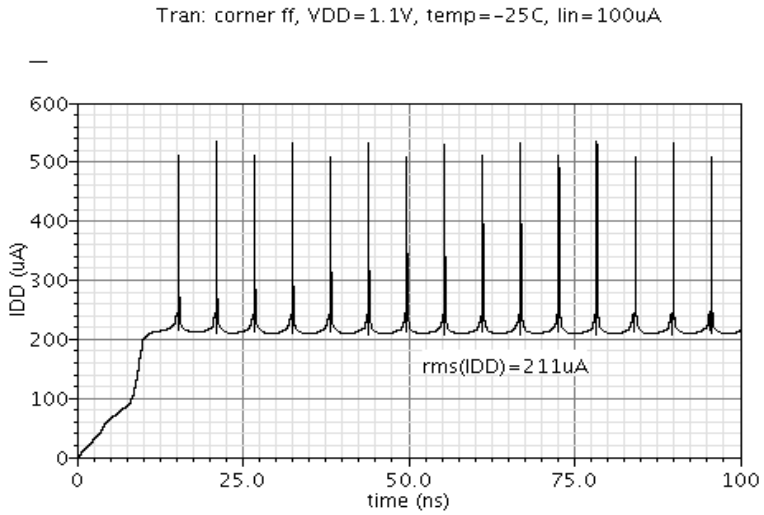

Fig. 9 – Current consumption.

4. Comparisons with Other Works

Comparisons with works referenced in this paper are given below.

Table 1
Comparisons

	This work	Azcona *et al.*, 2011	Valero *et al.*, 2011	Wang *et al.*, 2006	Yadav *et al.*, 2013
Process (CMOS)	65 nm	0.18 µm	0.18 µm	0.25 µm	65 nm
Supply	1.0 V	1.8 V	1.8 V	2.5 V	1.0 V
Input range	[0.1, 100] µA	[0.1, 1.6] V	[0.0, 1.2] V	[0.1, 0.8] V	[0.1, 22] µA
Output frequency	[0.1, 100] MHz	[0.1, 1.98] MHz	[0.1, 1.1] MHz	[52, 416] kHz	[4.3, 960] MHz
Conver.-gain	1 MHz/µA	1.2 MHz/V	861 kHz/V	520 kHz/V	43 MHz/µA
Rel. error	1.42%	4.8%	0.4%	1%	–
Temperature range	[–25, +125] ºC	[–40, +85] ºC	[–20, +120] ºC	–	[0, +70] ºC
Power cons.	232 µW	423 µW	400 µW	–	–

Current-to-frequency converters generally have output ranges much larger than voltage-to-frequency converters. Compared to (Azcona *et al*., 2011) and (Valero *et al*., 2011), the converter proposed in this paper has larger output range of 50.5 times and 91 times, respectively.

The current-to-frequency converter presented in (Wang *et al*., 2006) has an output range larger than that proposed here, but also high linearity errors. That circuit operates in a feedback configuration with a frequency detector in the negative feedback path.

The relative linearity errors of the circuit described in this paper are quite small, although not using any voltage reference and MIM capacitors. As the circuit is simple, the silicon area is relatively small.

The proposed converter does not contain any means to compensate PVT variations, but possibilities to do that exist.

5. Conclusions

A very simple current-to-frequency converter is described. It is designed in 65 nm CMOS standard process, using only MOS transistors and polysilicon resistors, and operates at 1.0 V nominal supply voltage. The linearity errors are less than 1.5 % over [0.1, 100] MHz output range. Simulations show that PVT variations change the conversion-gain of the converter but do not affect the linearity of transfer characteristic.

The proposed converter may be used for a variety of applications such as analog-to-digital converters, phase-lock loops, frequency synthesizers etc. When included in a feedback configuration, the influences of PVT variations on the conversion-gain will be compensated automatically by the system. Also, the converter can be used as current-controlled oscillator.

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CONVERTOR LINIAR CURENT-FRECVENȚĂ CU GAMĂ MARE DE IEŞIRE

(Rezumat)

Se prezintă un convertor liniar curent-frecvență care funcționează în intervalul de temperatură [–25º, +125] ºC, cu tensiune de alimentare de la 0.9 V până la 1.1 V. Circuitul este proiectat într-o tehnologie CMOS standard de 65 nm şi conține numai tranzistoare MOS şi rezistoare de polisiliciu. Nu sunt utilizate tensiuni de referință şi nici condensatoare speciale de tip MIM.

Domeniul de conversie a curentului de intrare este [0.1, 100] µA iar tensiunile dreptunghiulare generate la ieşire au frecvențe de la 100 kHz până la 100 MHz. Erorile relative de liniaritate sunt mai mici de 1.5%.

Simulările arată că variațiile procesului tehnologic, tensiunii de alimentare şi temperaturii modifică panta caracteristicii de transfer a circuitului dar nu afectează liniaritatea acesteia.

Circuitul propus are utilizări diverse: convertoare analog-digitale, circuite PLL, sintetizoare de frecvență.