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CMOS DELAY CELL WITH LARGE TUNING RANGE

BY

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Abstract. A current-controlled CMOS delay cell containing only MOS transistors is presented. The circuit is designed in 65 nm CMOS standard technology and operates in the temperature range [–30, +130] °C with supply voltage from 0.9 V to 1.1 V (1.0 V nominal value). The delay can be adjusted in a wide range, from 150 ps to 250 ns approximately. The silicon area occupied by the circuit is relatively small, about 73 μm^2. For input signals with a frequency of 1 GHz, the delay cell has less than 150 μA (rms) current consumption at rated operating conditions.

Key words: delay cell; wide tuning range; current-controlled; low voltage.

1. Introduction

Delay cells are used in applications such as oscillators (Chen *et al.*, 2005; Hwang *et al.*, 2004), delay-locked loops (Cheng *et al.*, 2007; Chung *et al.*, 2010; Lu *et al.*, 2009), phase-locked loops (Chung *et al.*, 2003), frequency synthesis (Turker *et al.*, 2011) and various control signal generators.

The delay produced by a particular delay cell can be fixed or adjustable; in the latter case there are coarse and fine tunings. Four delay cell schematics are shown in Fig. 1.

The fixed-delay cell in Fig. 1 *a* is used in (Chung *et al.*, 2010). Only negative transitions of the input signal “IN” are delayed, when both control

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signals “reset” and “FAST” are low; cascading of two such cells is needed to delay both negative and positive transitions. The delay is produced at internal node A by charging the intrinsic capacitor C_A with the leakage current of the PMOS transistor marked with a dashed rectangle. Transistor sizes determine the value of leakage current which also depends on process, voltage and temperature (PVT) variations.

The delay cell in Fig. 1 *b* (Hwang *et al.*, 2010) contains a transmission gate whose equivalent resistance is linearly tuned by means of two complementary voltages (the sum of control voltages is equal to supply voltage V_{DD}).

The delay cell in Fig. 1 *c* (Turker *et al.*, 2011) is based on DCVSL (Differential Cascode Voltage Switch Logic) topology. Tuning of delay may be obtained by injecting equal currents in nodes QP and QN. The capacitive loads connected to QP and QN are not shown in the figure. Two high-resistivity poly silicon resistors are used.

The schematic shown in Fig. 1 *d* represents a half delay cell with 2-bit control signals S_1 and S_0 (Cheng *et al.*, 2007). Through these bits the delay range can be switched by properly increasing of currents I_n and I_p.

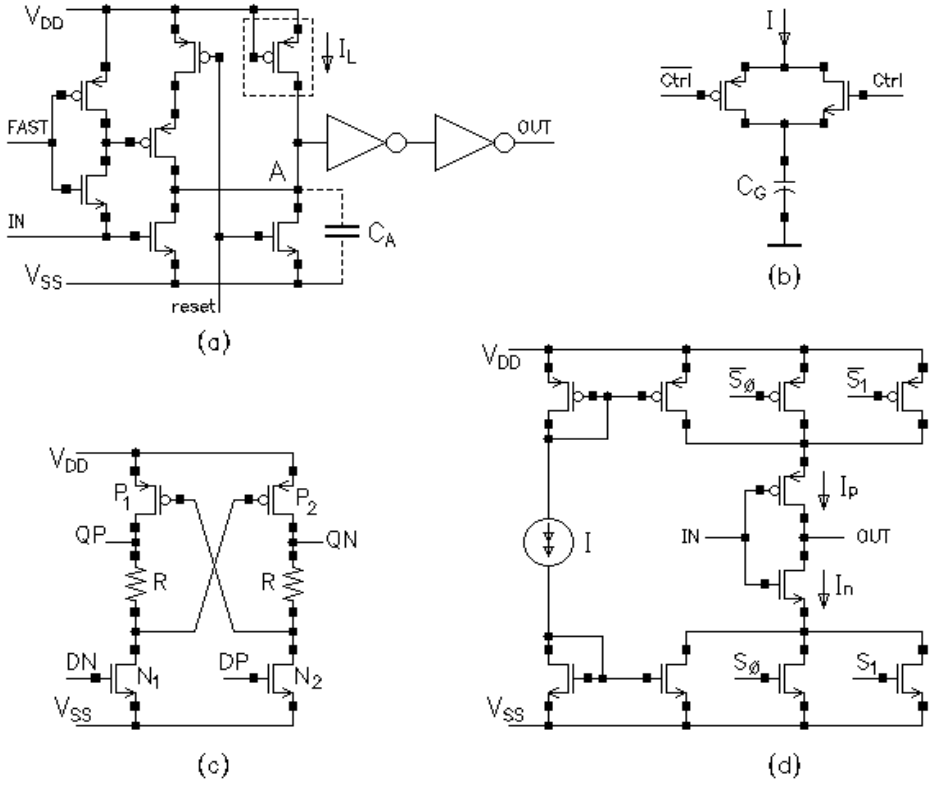

Fig. 1 – CMOS delay cells.

Other delay cells use NOR gates as a digitally controlled varactor for fine tuning (Chen *et al.*, 2005) or body-biasing technique to increase the tuning range (Lu *et al.*, 2009).

The delay cell proposed here is based on a Schmitt trigger with current-controlled threshold voltages, derived from the one described by Imbrea, (2015).

2. Circuit Description

The schematic of the proposed delay cell is shown in Fig. 2. All transistors are standard-V_t core devices. The capacitor C is made of one 2.5 V NMOS native transistor. All five logic gates are custom circuits, not standard library cells. The input and output of the circuit are V_{in} and V_{out}.

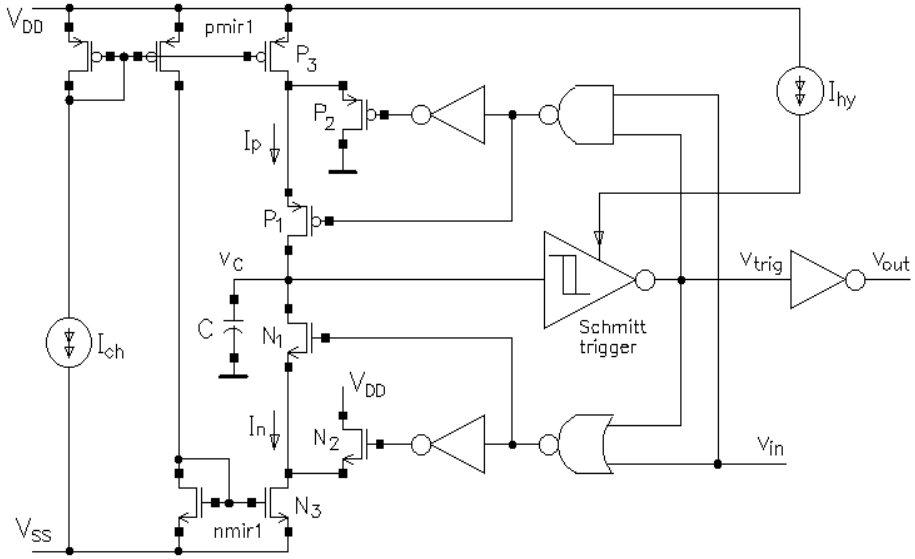

Fig. 2 – Schematic of the proposed delay cell.

There are two ways of tuning the delay, namely through the current I_{ch} (which controls the speed of charging/discharging the capacitor C) and through the current I_{hy} (which sets the threshold voltages V_{tL} and V_{tH} of the Schmitt trigger).

The voltage V_C across capacitor C is changing between V_{tL} and V_{tH}. A positive transition of V_{in} determines N_1 off, P_2 off and N_2 on, P_1 on. Capacitor C is charging by the current I_p (proportional to I_{ch}) and the voltage V_C increases from V_{tL} to V_{tH}. When V_{tH} is reached, the Schmitt trigger switches V_{trig} from high to low and a positive transition occurs at V_{out}. While V_{in} remains high, both transistors N_1 and P_1 are off ($I_n = I_p = 0$) and the capacitor C keeps V_C very close to V_{tH}. The outputs currents of mirrors "pmir1" and "nmir1" drain through P_2 on

and N_2 on, respectively. The delay between positive transitions of V_{in} and V_{out} is given by

$$\text{delay}_P \simeq \frac{V_{t\text{H}} - V_{tL}}{I_p} C \,. \tag{1}$$

A negative transition of V_{in} determines N_1 on, P_2 on and N_2 off, P_1 off. Capacitor C is discharging by the current I_n (proportional to I_{ch}) and the voltage V_C decreases from V_{tH} to V_{tL}. When V_{tL} is reached, the Schmitt trigger switches V_{trig} from low to high and a negative transition occurs at V_{out}. While V_{in} remains low, both transistors N_1 and P_1 are off ($I_n = I_p = 0$) and the capacitor C keeps V_C very close to V_{tL}. The outputs currents of mirrors "pmir1" and "nmir1" drain through P_2 on and N_2 on, respectively. The delay between negative transitions of V_{in} and V_{out} is given by

$$\text{delay}_N \simeq \frac{V_{t\text{H}} - V_{tL}}{I_n} C \,. \tag{2}$$

By properly sizing the transistors P_3 and N_3 we can get $I_n = I_p = \xi_1 \cdot I_{ch}$, where ξ_1 is a constant ($\xi_1 > 1$), and thus $\text{delay}_P = \text{delay}_N = \text{delay}$.

The trigger circuit is shown in Fig. 3. Thresholds V_{tL} and V_{tH} can be calculated using the following two formulas (Imbrea, 2015).

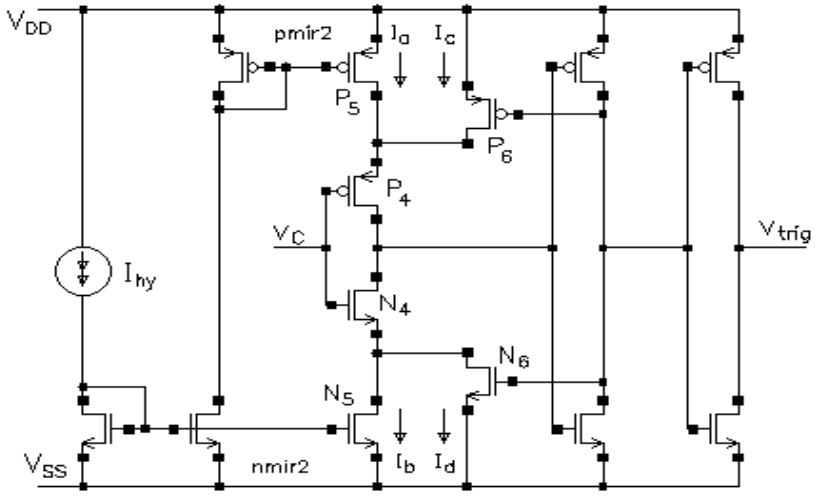

Fig. 3 – Schematic of the Schmitt trigger.

$$V_{tL} = V_{\text{thn}} + 2nV_{\text{T}} \ln\left(\exp\frac{\sqrt{I_a L_{\text{N4}}}}{V_{\text{T}}\sqrt{2n\mu_n C_{oxn} W_{\text{N4}}}} - 1 \right), \tag{3}$$

$$V_{tH} = V_{DD} - |V_{\text{thp}}| - 2nV_{\text{T}} \ln\left(\exp\frac{\sqrt{I_b L_{\text{P4}}}}{V_{\text{T}}\sqrt{2n\mu_p C_{oxp} W_{\text{P4}}}} - 1 \right). \tag{4}$$

The terms used in (3) and (4), namely $V_{thn(p)}$, V_T, n, $\mu_{n(p)}$, $C_{oxn(p)}$, and W/L have the meanings: NMOS (PMOS) threshold voltage, thermal voltage, slope factor, mobility of electrons (holes), gate-oxide capacitors per unit area, and channel width/length ratio, respectively.

Currents I_a and I_b are proportional to I_{hy}, so we can write $I_a = \xi_2 \cdot I_{hy}$, $I_b = = \xi_3 I_{hy}$, where ξ_2 and ξ_3 are constants. In order to obtain a simple formula for delay, we may size the transistors in Fig. 3 so that

$$(\xi_2 L_{N4})/(\mu_n C_{oxn} W_{N4}) = (\xi_3 L_{P4}) / (\mu_p C_{oxp} W_{P4}). \quad (5)$$

By combining the five equations above we get

$$\text{delay} = \frac{C}{\xi_1 I_{ch}} \left[V_{DD} - |V_{thp}| - V_{thn} - 4nV_T \ln\left(\exp \frac{\sqrt{\xi_2 I_{hy} L_{N4}}}{V_T \sqrt{2n\mu_n C_{oxn} W_{N4}}} - 1 \right) \right]. \quad (6)$$

Both currents I_{ch} and I_{hy} serve for tuning the delay, either coarse or fine. The delay can be adjusted in a wide range, depending on the input signal frequency, as shown in the next section.

3. Simulation Results

Delay values for input signals with different frequencies are illustrated in the following three figures. The threshold voltages of Schmitt trigger are also pointed out in each case.

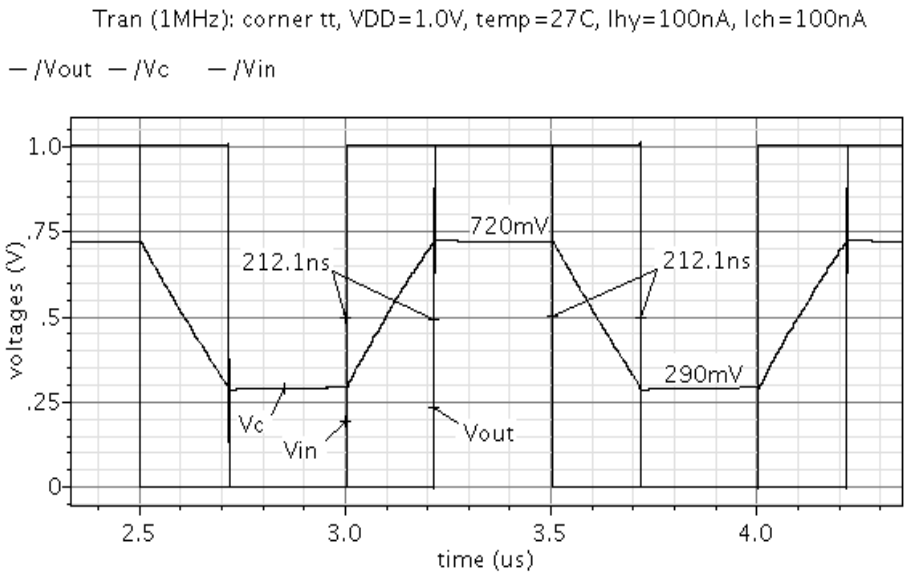

Fig. 4 – Delaying a signal of 1 MHz frequency.

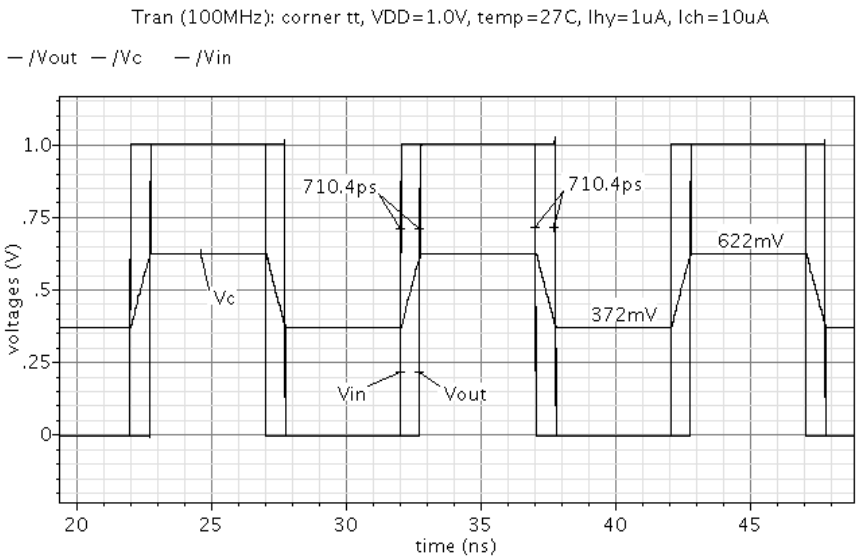

Fig. 5 – Delaying a signal of 100 MHz frequency.

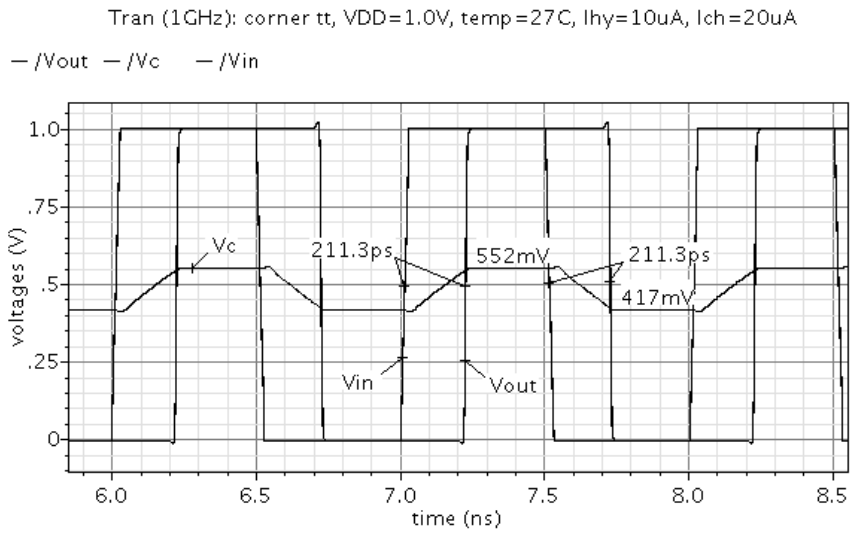

Fig. 6 – Delaying a signal of 1 GHz frequency.

As it can be seen from the above time diagrams, the delay of proposed circuit may be adjusted between large limits. The lower limit is about 150 ps and is determined by intrinsic delays of the circuit. The upper limit can exceed 250 ns and it is mainly determined by leakage.

For comparison, the cell in Fig. 1 *a* (Chung *et al.*, 2010) has a delay of 67.2 ns and that one used by Lu *et al.*, (2009) may be tuned in the range

[0.4, 1.9] ns. The delay cell in Fig. 1 *b* (Hwang *et al.*, 2010) has a large range of adjustment, similar to that of the cell proposed here. The others cells referenced in this paper have much smaller delays.

PVT variations affect the delay as shown in Figs. 7,…,9.

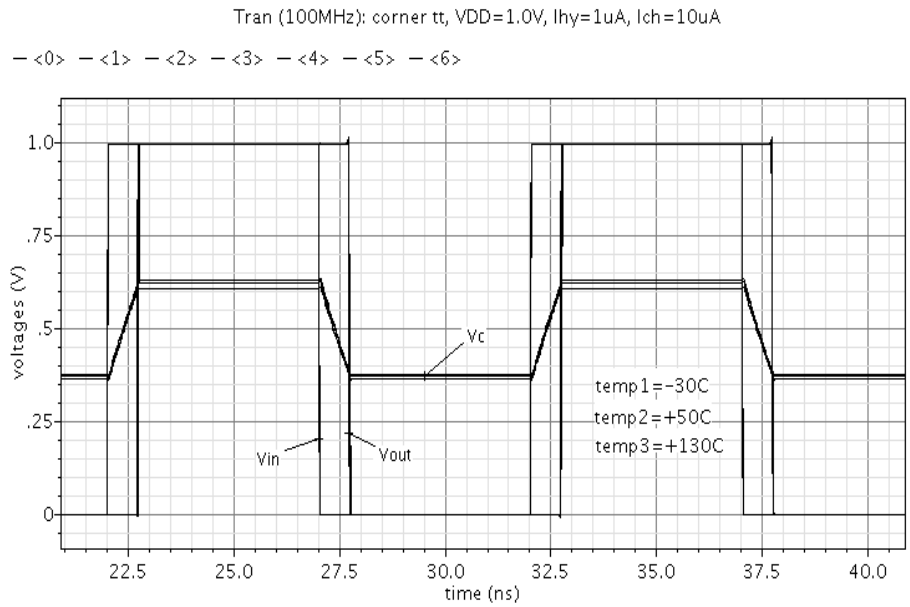

Fig. 7 – Influence of temperature on the delay.

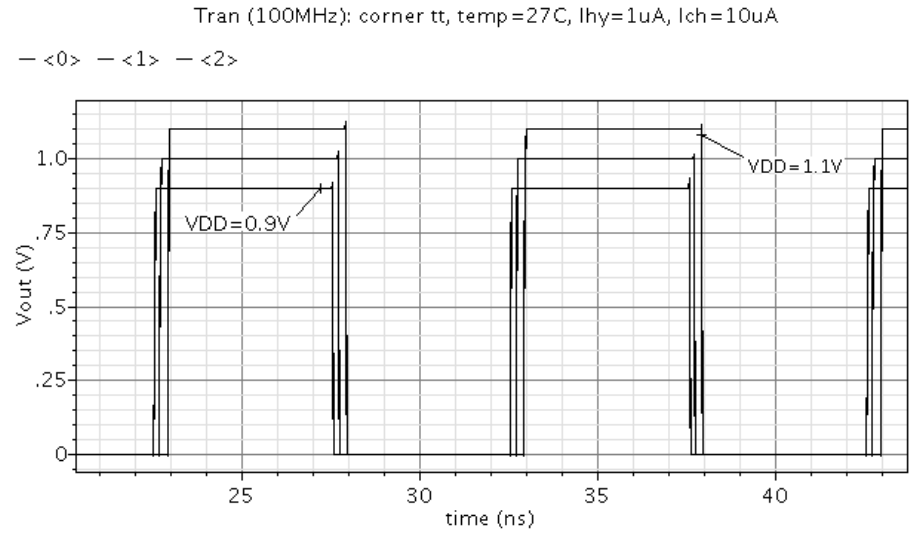

Fig. 8 – Influence of supply voltage on the delay.

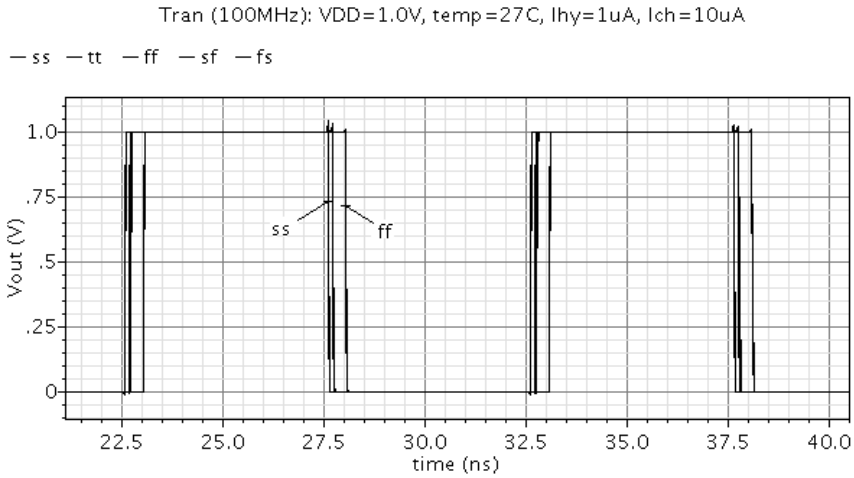

Fig. 9 – Influence of process corners on the delay.

The temperature has little influence on the delay (because $V_{thn(p)}$ and V_T have opposite temperature coefficients) but supply voltage and process affect it significantly. However this is not an issue, as the delay can be tuned by changing the values of control currents. In most applications the delay cell is included in feedback configurations and the adjustment is automatic.

Current consumptions of the proposed delay cell for two input frequencies, at rated operating conditions, are shown in Fig. 10.

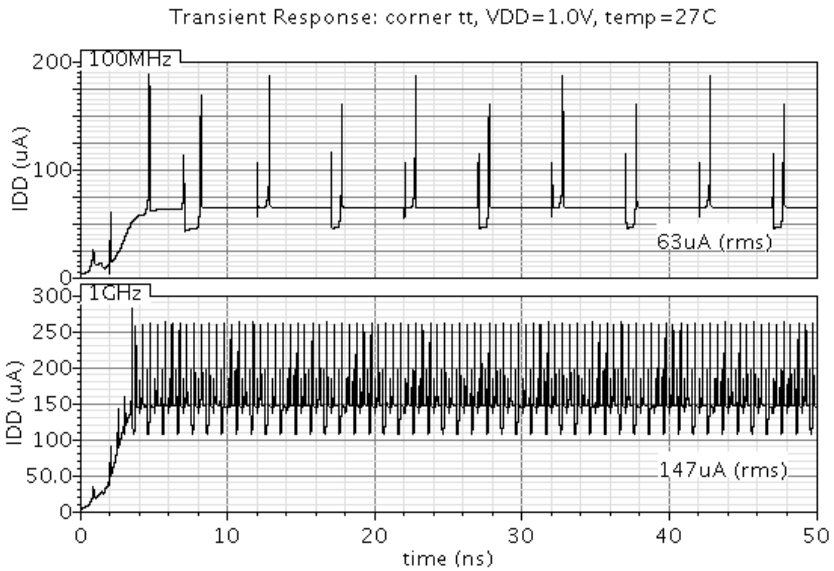

Fig. 10 – Current consumption.

The layout view of the proposed delay cell is illustrated in Fig. 11. Silicon area is relatively small (11.4 µm × 6.4 µm). This is approximately the area occupied by six simple D flip-flops (which belong to a standard library cell of 65 nm CMOS technology).

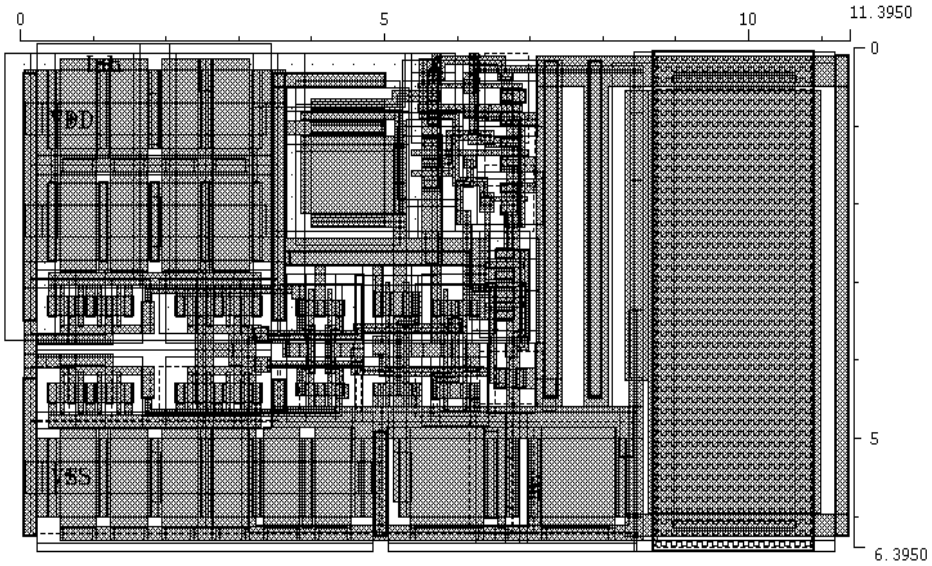

Fig. 11 – Layout of the proposed delay cell.

4. Conclusions

A CMOS delay cell with wide tuning range, from 150 ps to 250 ns, is described. The circuit contains only MOS transistors. The delay adjustment is achieved by means of two input currents that take values between 100 nA and 20 µA. One current controls the speed of charging / discharging a capacitor and the other sets the threshold voltages of a Schmitt trigger circuit. Silicon area and power consumption are relatively low.

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CELULĂ DE ÎNTÂRZIERE CMOS CU GAMĂ MARE DE REGLARE

(Rezumat)

Se prezintă un circuit de întârziere pentru semnale digitale care funcționează în domeniul de temperatură [–30º, +130] ºC, cu tensiune de alimentare de la 0.9 V până la 1.1 V. Circuitul este proiectat într-o tehnologie CMOS standard de 65 nm şi conține numai tranzistoare MOS.

Întârzierea poate fi reglată într-un interval mare [150 ps, 250 ns] prin intermediul a doi curenți; unul controlează viteza de încărcare/descărcare a unui condensator iar celălalt determină pragurile unui circuit de tip trigger Schmitt.

Circuitul ocupă o arie de siliciu de aproximativ 73 μm^2 si consumă 147 µA (rms) în condiții nominale de operare, pentru semnale de intrare cu frecvența de 1 GHz.

Celula de întârziere propusă se poate utiliza în aplicații diverse: circuite DLL, circuite PLL, sintetizoare de frecvență, oscilatoare, generatoare de semnale.