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TECHNIQUES TO REDUCE THE PARASITIC CAPACITANCE OF THE MULTILAYER SPIRAL INDUCTORS

BY

ADINA RĂCĂŞAN[*], CLAUDIA PĂCURAR, VASILE ȚOPA, CLAUDIA CONSTANTINESCU and SERGIU ANDREICA

Technical University of Cluj-Napoca, Romania
Department of Electrotechnics and Measurements

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Abstract. The paper presents new techniques to reduce the parasitic capacitance that appears with the transition from the monolayer spiral inductor to the multilayer spiral inductor, techniques that are proposed, analyzed and tested by the authors. The spiral inductors are used in integrated circuits, which in our days, tend to have the dimensions as small as possible and very high performance, for these reason is needed the transition to the use of the multilayer spiral inductor. The transition from the monolayer spiral inductors to multilayer ones leads to the increase of their inductances, which allows to reduce the area of spiral inductor, but this imply also the increase of the parasitic capacitances. To solve this disadvantage in this paper the authors propose some techniques to minimize the parasitic capacitance that appears once with the transition from monolayer to multilayer spiral inductors. The research effectuated confirms the efficiency of proposed techniques leading to a significant reduction of parasitic capacitance.

Key words: parasitic effects; multilayer planar inductor; numerical modeling; planar electromagnetic technology.

1. Introduction

The high evolution of technology in wireless communications and telecommunications and in radio frequency integrated circuits have generated

[*]Corresponding author: *e-mail*: Adina.Racasan@et.utcluj.ro

increased interest on these spiral inductors. For this reason their design and development tends toward robust and compact forms, innovative design, dimensions and weight as small as possible, raised reliability and performance, lower sale prices and production costs. Unlike the traditional spiral inductors, multilayer spiral inductors are ideal for a wide range of applications: PCB, SoC, integrated inductive and capacitive sensors (temperature, acceleration, biomedical, chemical sensors, etc.) and in wireless power systems of the various devices including medical (implants), as illustrated in Fig.1 (Avram *et al*., 2014; Ciupa *et al*., 2010; Iudean *et al*., 2014; Ng *et al*., 2010; Olivo *et al*., 2013; Păcurar *et al*., 2014; Păcurar *et al*., 2013; Răcăşan *et al*., 2014).

The objective of the paper aims both at presenting the advantages which appear with the transition from the monolayer spiral inductor to the multilayer spiral inductor, and also presenting and solving disadvantages, of which the most acute is created by parasitic effects which affects their performances. Thus, to obtain some configurations with maximum efficiency, in the second part of this paper is proposed and described techniques to minimize the parasitic effects.

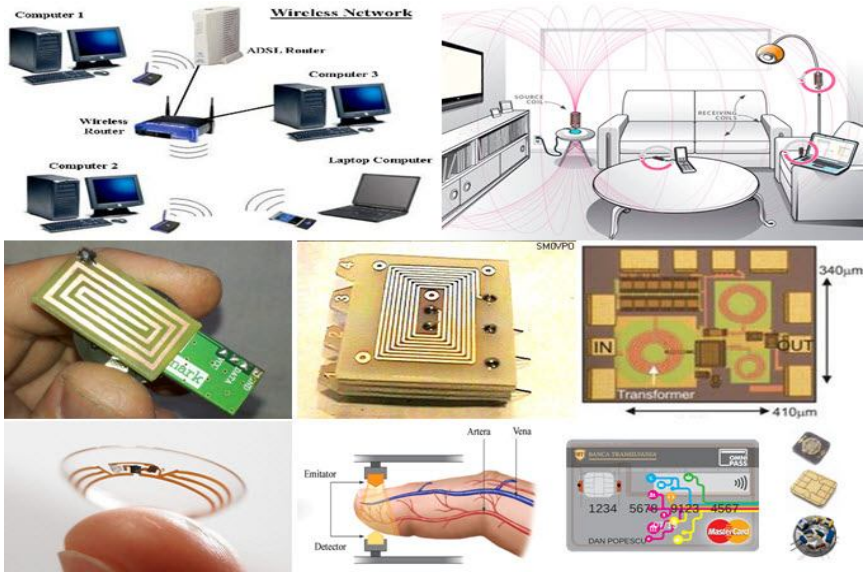


Fig.1 − Examples of integrated circuits and devices containing spiral inductors (Avram *et al*., 2014; Ciupa *et al*., 2010; Iudean *et al*., 2014; Ng *et al*., 2010; Olivo *et al*., 2013; Păcurar *et al*., 2014; Păcurar *et al*., 2013; Răcăşan *et al*., 2014).

2. Analyzing the Advantages and Disadvantages of the Multilayer Spiral Inductors

To analyze the advantages and disadvantages of the multilayer planar inductors we started from the monolayer inductors shown in Fig. 2 in which

both its components and its characteristic parameters may be identified, characteristic parameters which were analyzed in previous researches of the authors, as can be observed in Păcurar *et al*., (2013), Răcăşan *et al*., (2014). Thus it can be observed that the parasitic parameters are present in monolayer spiral inductors as well, but in the performed studies it can be noticed that they are more pronounced in multilayer inductors.

In order to achieve these research results, a set of multilayer circular spiral inductors was created. Then we have analyzed their configurations from 1 layer and then gradually increasing the number of layers of the copper inductor from 2 layers and up to 10 layers. The geometrical dimensions of the model are: the width of the turn, w is 10 µm, the distance between turns, s is 5 µm, thickness of the turn, t is 2 µm, the exterior diameter 500 µm, all this forming the planar spiral inductor. Silicon dioxide layer has a thickness of 10 µm and a width of 530 µm, is square shaped, and the silicon substrate has a thickness of 250 µm and a width of 530 µm, having a square shape.

In Fig. 3 is exemplified a spiral inductor with, 10 layers respectively 5 layers and 2 turns on each layer. This figure also presents how the connections between layers are made.

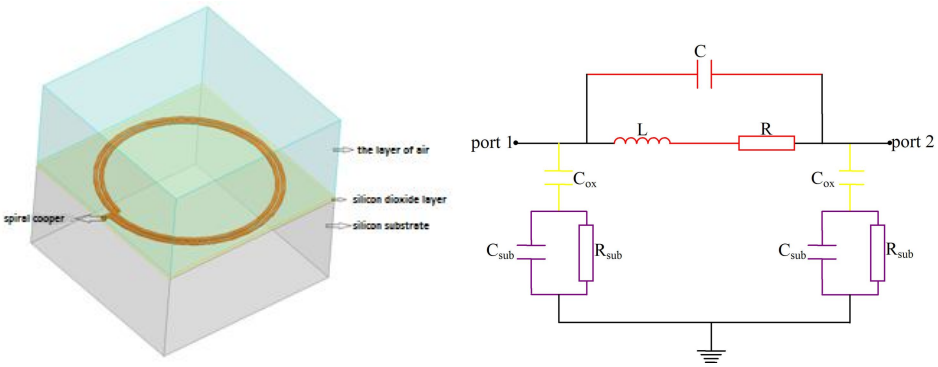


Fig. 2 – The equivalent circuit of monolayer spiral inductor.

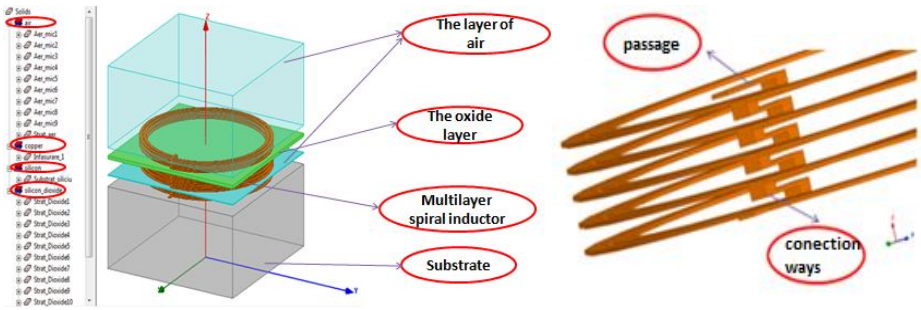


Fig.3 – Spiral inductor with 10 and 5 layers, each layer having 2 turns.

The electrical parameters of the spiral inductors that are detailed in Fig. 2 are: spiral inductance (L), spiral resistance (R) and spiral capacitance (C); oxide capacitance (C_{ox}), substrate resistance (R_{sub}) and substrate capacitance (C_{sub}).

The determination of the parameters for the developed inductors was performed by means of a commercial software program by creating 10 independent projects, one for each type of inductor proposed. It must be mentioned that in the numerical modeling of the spirals that form the multilayer inductors the considered material is copper. The inductor is placed on the silicon dioxide layer having the relative permittivity 4, and then the oxide layer is placed on the silicon substrate with the relative permittivity 11.9. In order to show that the transition from monolayer spiral inductors to multilayer spiral inductors leads to an increase of inductance value, the results obtained for all 10 types of inductors have been centralized and presented in Fig. 4. This figure shows the variation of inductance depending on the number of layers of the inductor and also depending on the frequency for the case the inductor with two turns for each layer. As can be observed, the inductance increases both with the increased of the layers number, and also with the frequency increased.

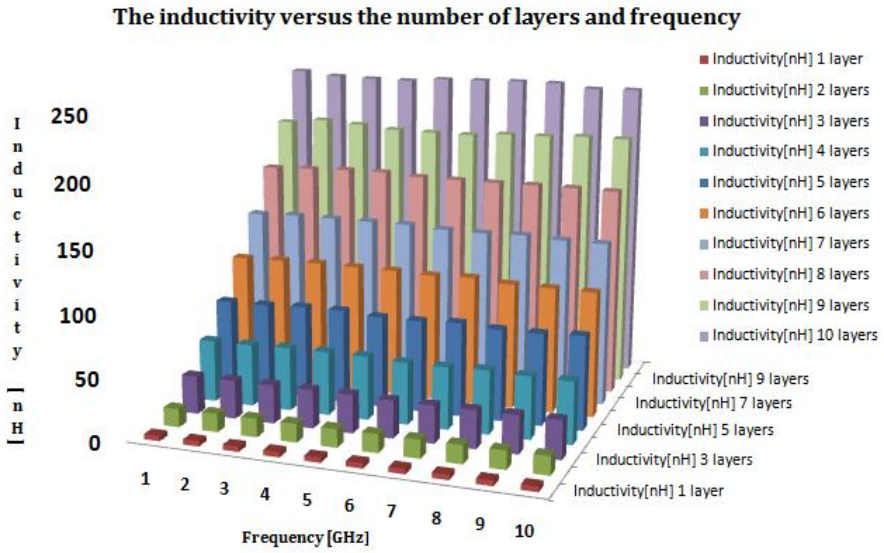


Fig. 4 – Variation of inductivity versus the number of layers and frequency for the multilayer inductors with 2 turns per layer.

In Fig. 5 the parasitic capacitance values, obtained for two of the inductors proposed by the authors are presented the capacitance matrix obtained in the case of the two layers inductor with two turns on each layer, and the capacitance matrix of the inductor obtained with 10 layers and two turns on each layer.

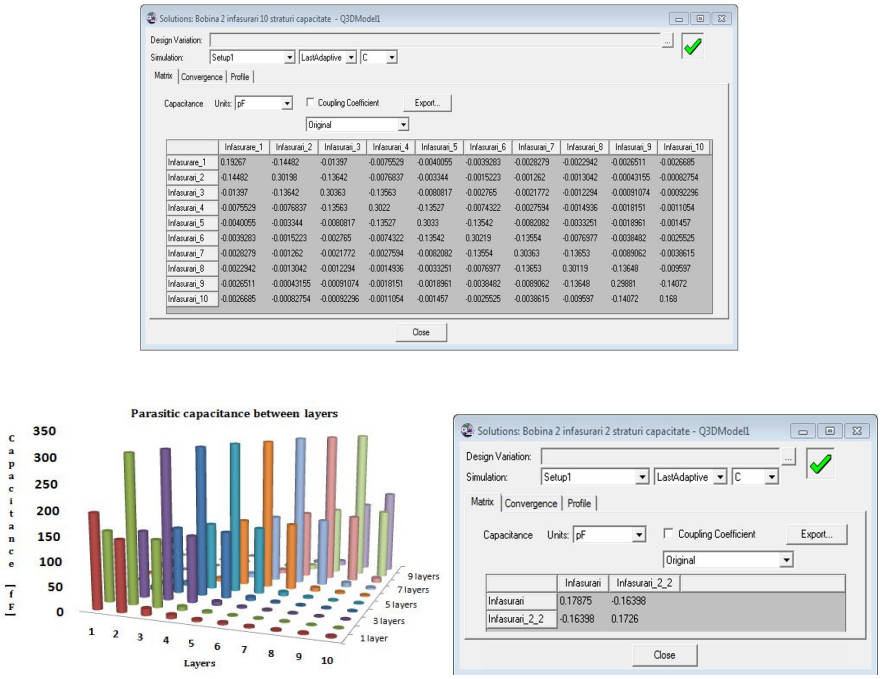


Fig. 5 – Parasitic capacitance located between the layers that form the multilayer inductor with 2 turns per layer.

To be able to interpret more easily the obtained results, they are represented in graphical form the matrix with 10 layers and two turns on each layer. It can be observed that the parasitic capacitance is maximum between the central copper layers of the inductor and by increasing the distance between the layers the value of the parasitic capacitance decreases. It mentioned the fact that for the monolayer inductor the obtained inductance value is 4.22 nH and the parasitic capacitance is 22.33 fF.

3. Techniques to Minimize the Parasitic Effects of the Multilayer Spiral Inductors

From the results obtained by numerical modeling of the 10 types of multilayer spiral inductors, shown in Fig. 4 and respectively in Fig. 5, it can be noted that the inductance of the inductors greatly increases with the transition from the monolayer spiral inductor to the multilayer spiral inductor, but, as we expected, the parasitic effects also increase a lot, more specifically the value of the parasitic capacitance between layers of copper that make up the multilayer inductor. Thus, further some solutions are proposed to minimize these parasitic effects that appear with the transition from the monolayer spiral inductor to the multilayer spiral inductor.

3.1. The Influence of the Type of Material from which the Oxide Layer is Made on the Parasitic Capacitance

The researches were carried out on the same set of inductors proposed in the previous paragraph, namely, the circular multilayer spiral inductors with 2 turns and the number of layers varying from 1 to 10. This case analyses the influence of the type of material of which the oxide layer is made on the parasitic capacitance between the layers of copper which compose multilayer inductor on the inductance of the multilayer circular spiral inductors. More exactly, by changing the type of material used for the oxide layer we aim to minimize the parasitic capacitance and at the same time to keep a high value of the inductors inductance. Materials used for the oxide layer in the present study are: silicon dioxide (ε_r = 4), epoxy Kevlar (ε_r = 3.6), Rogers RO3003 (ε_r = 3), glass PTFE (ε_r = 2.5), Duroid (ε_r = 2.2).

All of the 10 types of inductors proposed were analyzed. Fig. 6 shows the results for the parasitic capacitance obtained in the case of the inductor with 2 layers and 2 turns on each layer depending on the different types of materials used for the oxide layer. To show that the proposed solution is totally reliable for inductors with more than two layers, a series of selective results are presented in Fig. 7 describing the case of the inductor with 5 layers / 2 turns.

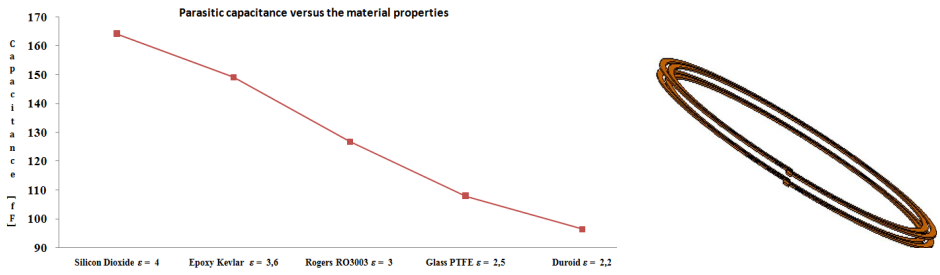


Fig. 6 – Parasitic capacitance values depending on the type of material used for the oxide layer in the case of the two layers inductor.

Therefore, the results presented in Figs. 6 and 7 confirm that the solution proposed by the authors lead to minimizing the parasitic capacitance that occurs with the transition from the monolayer spiral inductors to the multilayer spiral inductors. Table 1 presents the inductance values obtained for some of the 10 types of multilayer spiral planar inductors that were proposed by the authors, depending on the material used for the oxide layer. Analyzing the inductance values obtained for different types of materials used for the oxide layers one can observe that the proposed solution does not affect the inductor

inductance values it retains the initial value and in some cases even leads to an increase of the initial value.

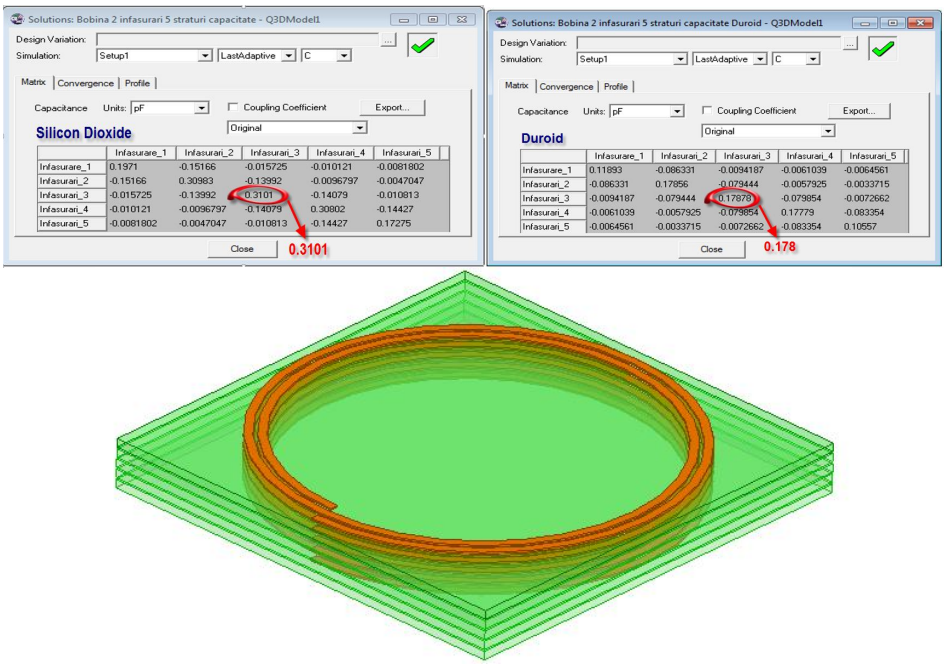


Fig.7 – Parasitic capacitance values depending on the type of material used for the oxide layer in the case of the five layers inductor.

Table 1
The Values of the Inductivity for the Multilayer Inductor Depending on the type Oxide Layer Used

Number of layers	*1*	*2*	*5*	*10*
Inductivity, nH, Silicon Dioxide	4.22	14.86	74.28	237.73
Inductivity, nH, Epoxy Kevlar	4.22	15.01	76.44	241.49
Inductivity, nH, Rogers RO3003	4.22	14.94	74.47	241.49
Inductivity, nH, Glass PTFE	4.22	14.94	74.47	241.49
Inductivity, nH, Duroid	4.22	15.00	74.47	241.49

3.2. The Influence of the Distance between the Copper Layer that make up the Multilayer Inductor on the Parasitic Capacitance

Next, the influence of the distance between copper layers that make up the multilayer spiral inductor on its parameters was analyzed, aiming this time to minimize the parasitic capacitance between the inductor's layers and at the same time maintaining a high inductance value. For this analysis the distance between inductor layers was varied from 10 to 20 μm. The analyzes were

performed for all 10 types of multilayer inductors proposed using the initial structures, which are presented in the second paragraph in which the oxide layer is made out of silicon dioxide. As an example, Fig. 8 shows the results for the parasitic capacitance obtained in the case of the inductor with two layers having two turns on each layer depending on the distance between the layers. It can be observed that the parasitic capacitance decreases with the increase of the distance, as we expect. The analyzes of the influence of distance between the copper layers and its effects on inductor's inductance can be done using experimental data presented in Table 2.

Table 2

The Values of the Multilayer Inductor's Inductivity Depending on the Distance Between the Layers that form the Inductor

Distance, [µm]	*10*	*15*	*20*
Inductivity, [nH]	14.69	13.99	13.92

It is assessed that this solution minimizes the parasitic capacitance that leads to small changes in the value of the inductor's inductance.

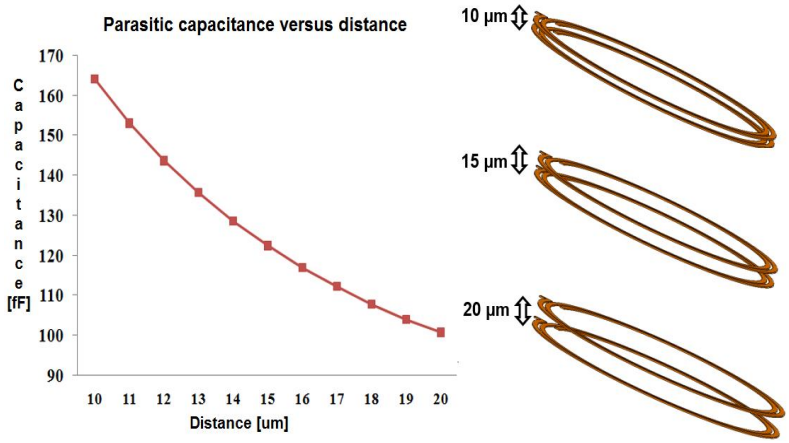


Fig. 8 – Parasitic capacitance values depending on the distance between the layers that form the multilayer inductor in the case of the two layers inductor.

3.3. The Influence of the Placement of the Copper Layers that Make up the Multilayer Inductor on the Parasitic Capacitance

In research results presented in the previous paragraphs, the copper layers that form the multilayer inductor have been symmetrically placed relative to each other; each spire of a layer is located just above the up or down turn's layer, of course being separated by the silicon dioxide layer. Next, it is proposed to analyze the case in which the placement configuration of the odd layer conductors is changed, a shifting being applied, in order to increase the diagonal

distance between the layer's turns, as shown, for example, in Fig. 9 in the case of two inductors on two layers inductor with 5 turns on each layer.

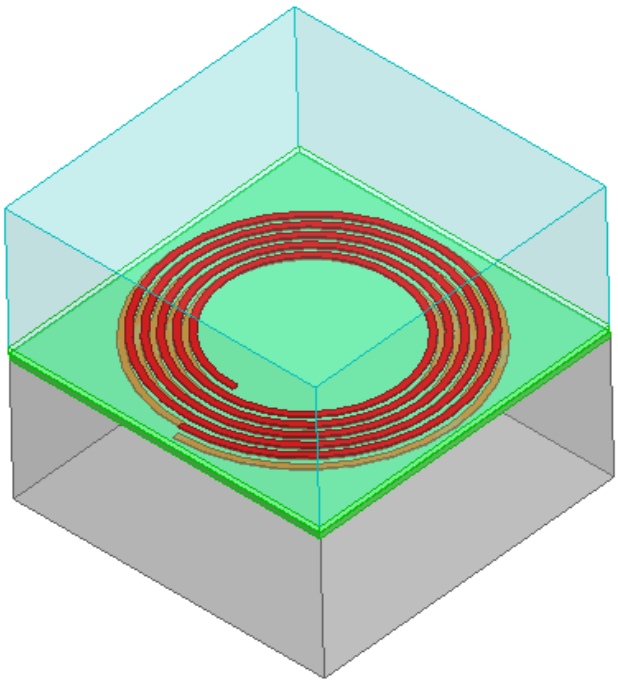


Fig. 9 – Spiral inductor on 2 layers with 5 turns on each layer having the first layer staggered from the second layer.

In the image from Fig. 9 the shifting between the two copper layers of the multilayer inductor can be observed, shifting succeeding to change the distance on diagonal, between conductors of the two layers that form the analyzed inductor. Fig. 10 shows the variation of the parasitic capacitance obtained for the inductor with 2 layers / 2 turns on each layer for different assigned shifting of the first layer's conductors.

The way the shifting is influencing the inductance of the analyzed inductor is presented in Table 3. Therefore, analyzing the results presented in Fig. 9 and in Table 3 the efficiency of the shifting method proposed to minimize parasitic capacitance is assessed.

Table 3
Values of the Multilayer Inductor Inductivity Depending on the Shifting Attributed

Shifting, [μm]	*1*	*5*	*10*
Inductivity, [nH]	14.69	14.66	14.58

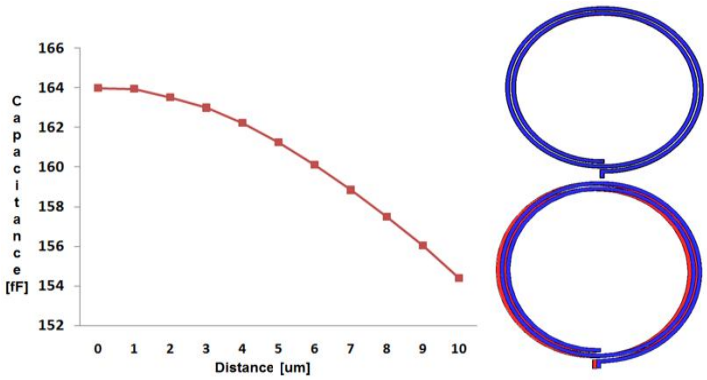


Fig. 10 – Parasitic capacitance values depending on the shifting attributed to the first layer conductors of the inductor with two layers.

3.4. The Efficiency of the Proposed Solutions for Minimizing the Parasitic Capacitance of the Multilayer Inductors

In order to show that the solutions proposed by the authors for minimizing the parasitic capacitance of multilayer inductors are efficient in the case of multiple turns, the inductors on 5 layers with 6 turns on each layer, with circular form and square form are presented in Figs. 11 and 12. In both figures are presented the capacitance matrix obtained for the initial case in which the turns are placed symmetrically on silicon dioxide layers. The inductance obtained for multilayer inductor with circular form is about 416 nH, respectively 498 nH for multilayer inductor with square form. One can observe by comparing the inductance values obtained for the two forms that they are slightly different, caused by the end and proximity effects, which differ from one form to another.

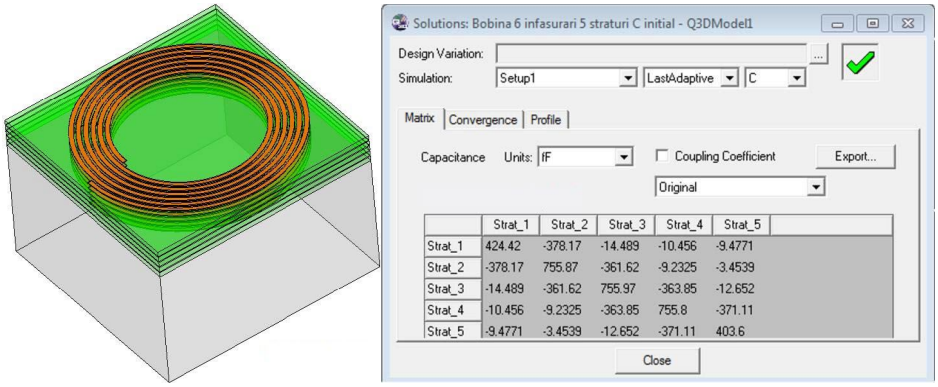


Fig.11 – Parasitic capacitance values in the case of the inductor on 5 layers with 6 turn on each layer with circular form - initial configuration.

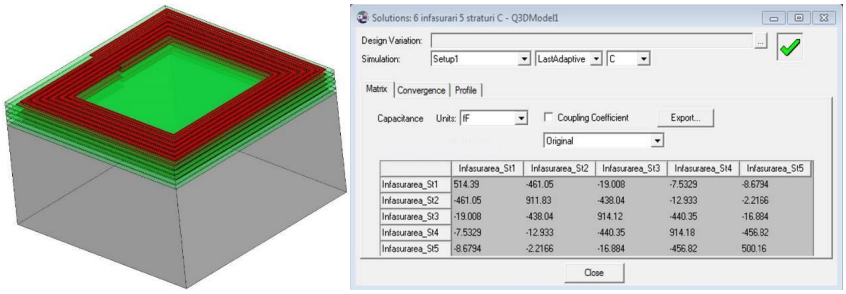


Fig. 12 – Parasitic capacitance values in the case of the inductor on 5 layers with 6 turn on each layer with square form - initial configuration.

Considering the results and conclusions of the presented studies in previous paragraphs, next the solutions proposed to minimize the parasitic capacitance will be applied to the inductor with 5 layers and 6 turns on each layer. Therefore, a multilayer inductor will be built in which the turns of the inductor will be placed on layers of duroid, the thickness of the two layers of duroid from the vicinity of the central layer will be increased, and the conductors from the odd layers of the inductor will be attributed to a shifting of 10 μm. In Fig. 13 is presented an image describing the configuration proposed for the inductor with 5 layers and 6 turns on each layer, with circular form and the capacitance matrix obtained in this case. In Fig. 14 is illustrated the same images but for multilayer inductor with square form. The inductance value obtained for multilayer inductor with circular form is about 386 nH, respectively 460 nH for multilayer inductor with square form.

Analyzing the obtained results, it can be observed that the solutions proposed by the authors to minimize the parasitic capacitance in the case of the inductor on 5 layers with 6 turns per layer lead to its reduction to less than half, both for multilayer inductor with circular form and the same results for square form, thus showing the efficiency of the proposed solutions.

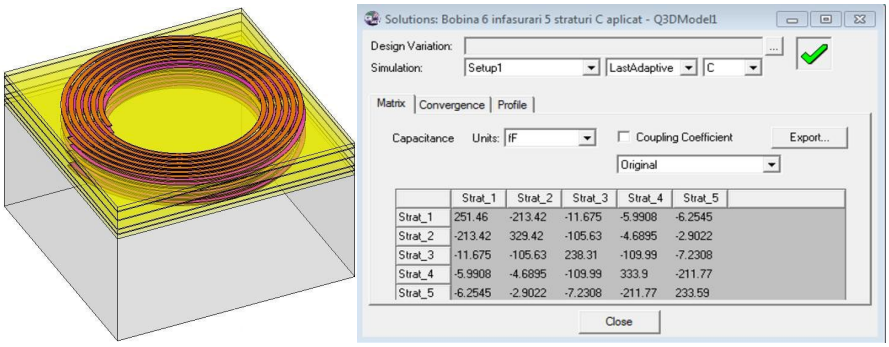
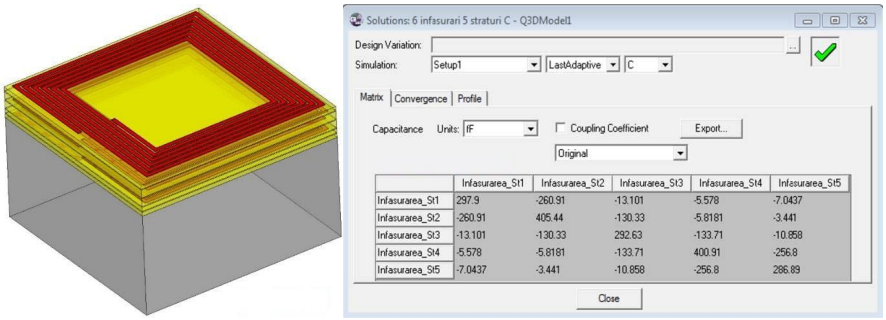


Fig. 13 – Parasitic capacitance values in the case of the inductor on 5 layers with 6 turn on each layer with circular form - the proposed configuration.



	Infasurarea_St1	Infasurarea_St2	Infasurarea_St3	Infasurarea_St4	Infasurarea_St5
Infasurarea_St1	297.9	-260.91	-13.101	-5.578	-7.0437
Infasurarea_St2	-260.91	405.44	-130.33	-5.8181	-3.441
Infasurarea_St3	-13.101	-130.33	292.63	-133.71	-10.858
Infasurarea_St4	-5.578	-5.8181	-133.71	400.91	-256.8
Infasurarea_St5	-7.0437	-3.441	-10.858	-256.8	286.89

Fig. 14 – Parasitic capacitance values in the case of the inductor on 5 layers with 6 turn on each layer with square form - the proposed configuration.

4. Conclusions

Analyzing the results obtained on the researches done on planar spiral inductors can be observed that the inductors' inductance increases very much once with the transition from monolayer to multilayer spiral inductors, but, as we expected, increase very much also the parasitic effects, more exactly the value of the parasitic capacitance between the cooper layers that composed the multilayer inductor. To solve these problems the authors proposed some techniques to minimize the parasitic effects that appear once with the transition from monolayer to multilayer spiral inductor.

So, by analyzing the influence of the type of material from which the oxide layers are made on the parasitic capacitance can be noted that the small capacitance is obtained in the case of the use of duroid material.

It is proposed and next analyzed the technique to reduce the parasitic effects by the configuration of the geometrical placement of the conductors that form the multilayer inductors. Because it was noted that the parasitic capacitance is bigger in the area of central layers that composed the inductor it is proposed to increase the distance between these layers. Also, was proved to be very efficient the shifting of conductors of the odd (or even) layers of the inductor, by this technique increasing the distance on the diagonal between the conductor of neighboring layers of the inductor.

The efficiency of the proposed solutions was tested in the final part on more complex configurations, namely on a circular spiral inductor, respectively on a square spiral inductor with 5 layers and 6 turns on each layer. The obtained results confirm the fact that the techniques proposed by the authors lead to the minimization of the parasitic capacitance that appear once with the transition from monolayer to multilayer spiral inductors.

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TEHNICI DE REDUCERE A CAPACITĂŢII PARAZITE DIN BOBINELE SPIRALĂ MULTISTRAT

(Rezumat)

Sunt prezentate noi tehnici de reducere a capacităţii parazite, care apare odată cu trecerea de la realizarea bobinelor spirală pe un strat la cele pe mai multe straturi, tehnici propuse, analizate şi testate de către autori. Bobinele spirală sunt utilizate în circuite integrate care, în zilele noastre, tind să aibă dimensiuni cât mai mici şi performanţe cât mai mari, astfel necesitatea utilizării bobinelor spirală multistrat este tot mai strigentă. Trecerea de la bobinele monostrat la cele multistrat conduce la creşterea inductivităţii acestora ceea ce permite micşorarea ariei necesare bobinei spirale, insă implică si creşterea capacităţii parazite. Pentru soluţionarea acestui dezavantaj în cadrul acestei lucrări autorii propun câteva tehnici de minimizare a capacităţii parazite care apare odată cu trecerea de la bobinele spirală monostrat la cele multistrat. Cercetările efectuate confirmă eficienţa tehnicilor propuse conducând la o diminuare semnificativă a capacităţii parazite.