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DUAL BAND IMPLEMENTATIONS OF LOW NOISE AMPLIFIERS IN CMOS TECHNOLOGY

BY

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Abstract. The increasing demand for multi-standard transceivers in mobile communications and terminals imposes multi-standard capability for low noise amplifiers, as well. This paper reviews the main techniques used to implement dual band CMOS low noise amplifiers, as reported in literature. Such amplifiers are sufficient to address a mobile standard, usually with two distinct frequency bands allocated to the transmitter and receiver, address two distinct wireless standards, such as WLAN (2.4 GHz and 5 GHz), or even a mixing between these two cases (a mobile frequency band – uplink or downlink - and one wireless standard). As can be noticed, most of these architectures are implemented with common source input stage while the multi-standard capability is achieved be means of LC resonant cells (series and parallel tanks). Due to length constraints, concurrent architectures only are covered in this article.

Key words: CMOS; dual-band; low noise amplifier; RFIC.

1. Introduction

Low noise amplifiers (LNA) represent key components in RF receivers, being the first active block after antenna on the RF path. They should be

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designed with power gain as high as possible and noise figure as low as possible. This way, the LNA would increase the signal power level received by the antenna while minimizing the noise figure produced by the following mixers. In addition, the proliferation of multi-standard devices imposes new constraints to LNA design, multi-standard LNAs being currently under development, either designed for particular frequency bands or with wideband capability.

A comprehensive study of dual band LNAs reported so far in the literature concluded with the idea that the best classification of these topologies should focus on how the multi-band frequency response was implemented. In this regard, there are two possibilities to design such low noise amplifiers: either covering two frequency bands simultaneously or switching the frequency band to the second one of interest. This article follows this point of view, being entirely dedicated to concurrent LNAs.

2. Concurrent Dual Band CMOS LNA

Concurrent dual band LNAs are amplifiers working at two frequencies simultaneously, without any tuning capability. Such amplifiers are usually implemented with a single stage consisting of two transistors, one being the common source input transistor and the second one a cascode transistor, generally used to increase the output resistance and therefore minimizing the reverse gain (or S_{12} equivalently) which can deteriorate the amplifier stability otherwise. A single stage signifies not only a more compact design and low chip area but also low power consumption and lower noise figure. However, simplifying the design of the active area translates the implementation of dual band function to the passive level, at both input and output, therefore imposing a trade-off between chip area, power consumption, linearity, noise figure and impedance matching.

The basic topology of such CMOS dual band amplifier is shown in Fig. 1 *a* (Hashemi & Hajimiri, 2001), where the input stage is not shown. Dual band function signifies, particularized to this concurrent LNA, allowing the frequencies of interest to pass through the amplifier while the out-of-band frequencies are rejected (or blocked). Such operation requires simultaneous filtering and impedance matching at the frequencies of interest, not easy to implement taking into account the chip area constraints and noise figure sensitivity with respect to the input impedance. The original solution shown in Fig. 1 *a* makes use of a LC parallel tank in series with a series inductor (bond wire in some cases) at the input port, for impedance matching purpose. To ensure maximum gain at two frequencies, a series LC tank (C_1, L_1) is added in parallel to the classical LC parallel tank (C_2, L_2), quite complicated formulas being used to size all 4 components. The idea with inserting the series tank is to create a notch characteristics at a particular frequency, freely chosen between the two frequencies of interest. The amplifier proposed in this reference has been designed in 0.35 μm CMOS process and proved a dual band capability at 2.45 GHz and 5.25 GHz (Hashemi & Hajimiri, 2002).

Three other similar concurrent dual band LNAs, covering the same frequency bands, have been reported for 0.25μm CMOS process (Feng & Shi, 2003; Jou *et al.*, 2003) but with a lower figure of merit (if computed), while 0.18μm CMOS process was also reported (Zhang *et al.*, 2003) with 2.5 dB noise figure.

The same topology was reported for a concurrent dual band LNA covering GSM 900 and Bluetooth (2.4 GHz) applications (Datta *et al.*, 2010a), these results being reported twice (Datta *et al.*, 2010b).

Another concurrent dual band amplifier working at 2.6 GHz and 5.25 GHz has been reported for 0.18μm CMOS process (Zhiqiang *et al.*, 2011) with good noise and power consumption performances (at least in simulations).

The same basic topology was used to design a dual band LNA (Zhang *et al.*, 2003) implemented in a 0.18μm CMOS process and covering 2.4 & 5.2 GHz bands. It exhibits voltage gains of 16 & 22.5 dB and NF of approximate 3 dB (3 dB, 3.1 dB) at these frequencies. The same frequencies were targeted by another similar implementation (Lee & Lin, 2004), the circuit being implemented in similar technology and providing 3 dB noise figure for 3 mW power consumption only.

An interesting approach (Kargaran & Madadi, 2010) consists of inserting a third transistor, M_2 as illustrated in Fig. 1b, with simultaneous splitting of the signal path so that M_2 amplifies the signal as well, being used as common source stage. The output transistor M_c still has both LC tanks for matching purpose (as in Fig. 1a). This method increases the overall gain while decreasing the noise figure. The amplifier was designed to cover both WiFi bands (2.4 & 5.2 GHz) and proved a noise figure as low as 2.5 dB at both frequencies while the gain was 20 dB (2.4 GHz)/12 dB (5.2 GHz).

A variation for this basic concurrent topology (Shouxian M. et al., 2003a) avoids inserting the series LC tank to the drain of M_c, the multi-band behavior being limited to the input matching network. However, a second stage is inserted for a plus in terms of gain (as shown in Fig. 2 *a*). The amplifier covers GSM 1800 and WLAN 5.8 GHz, being designed in a 0.25μm CMOS process. The same topology was used by the same authors to implement a dual band LNA covering:

a) 2.35-2.6 GHz and 5-6 GHz frequency bands (Shouxian *et al.*, 2003b);

b) GSM900 (935,…,960 MHz) and 1.8,…,2.5 GHz (GSM1800, DECT, PHS, PCS, WiFi/Bluetooth) frequency bands, mixing narrow band with wideband frequency response for the amplifier (Shouxian *et al.*, 2003c).

Another interesting variation (Hyvonen *et al.*, 2005) shown in Fig. 2 *b* makes use of two distinct series LC branches connected in parallel to the output node, each one allowing a frequency of interest (2.45 & 5.25 GHz).

Another variation (Shouxian *et al.*, 2004) avoids inserting the series LC tank to the drain of M_c, therefore moving the filtering operation completely to the input where a dual band selective network is used, consisting of two parallel LC tanks connected in series. The main advantage is the lower chip area due to lack of passives, L_s not being necessary while the pair L_1-C_1 is not used. However, the price is a supplementary power consumption due to the presence

of the output buffer, used as a second stage for matching purpose (good wideband impedance matching). The circuit was implemented in 0.18μm CMOS process, covers 2.4 & 5.6 GHz bands, proves a minimum gain of 10 dB and minimum noise figure of 3.6 dB for 18 mW power consumption. The same principle was used to implement a LNA covering 0.9/2.4 GHz bands (Datta *et al.*, 2010c). This amplifier was designed in a 0.13μm CMOS process and proved 1.9 dB noise figure, at least in simulations.

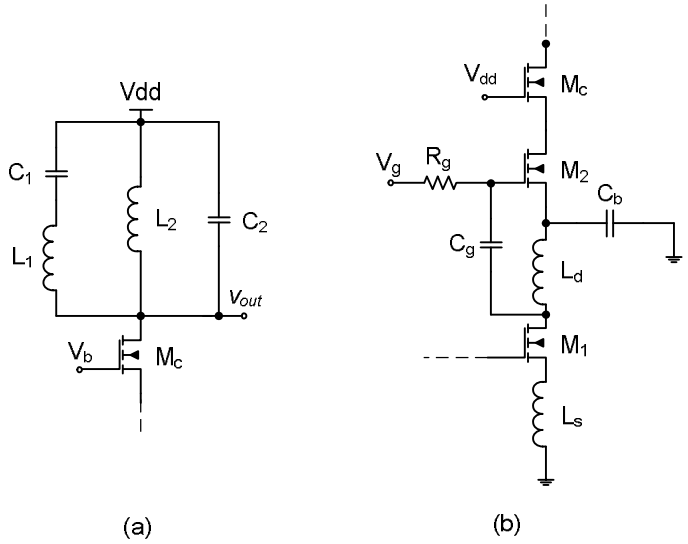

Fig. 1 – Output load for the basic topology of concurrent dual band LNA (*a*) and current reuse topology (*b*).

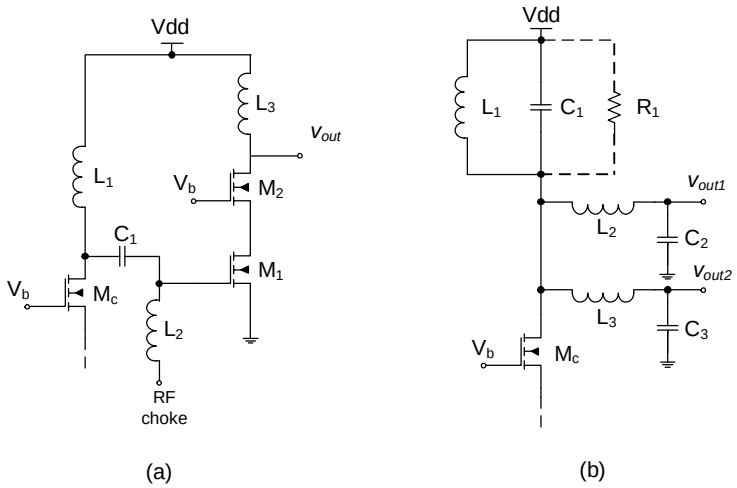

Fig. 2 – Modified topologies of concurrent dual band LNA with supplementary active stage (*a*) and two series LC branches (*b*).

By far a much more complicated dual band LNA (Gao *et al*., 2007) makes use of current reuse principle, active inductor for notch implementation to reject the 5 GHz component, wideband input matching together with shunt feedback resistor (similar to the cascode transistor) and series shunt peaking inductors for increased gain within the lower band. The amplifier, designed in a 0.18μm CMOS process, addresses UWB standard implementations, covering the first spectrum part (3,…,5 GHz) as well as the upper part (6,…,10 GHz). NF_{min} is 4 dB for a power consumption of 24 mW.

Another variation (Jhon *et al*., 2007), highly original and addressing microwave applications, covers the ISM bands 19 GHz and 25 GHz. It consists of implementing the LNA as distributed amplifier, with 3 identical common source transistors, cascaded by means of transmission lines. In addition, the amplifier uses a positive feedback loop, with L-C ladder networks, shown in Fig. 3 *a*, which are built from two cascaded PI LC networks (used for impedance matching). There are two ladder networks, one connected to the gates of all transistors and another one connected to the drain (load) inductors of these transistors. The amplifier was designed in 0.18 μm CMOS process, exhibits moderate gain of 8 and 11 dB at the two frequencies of interest and has a noise figure of approximately 6 dB for 8 mW power consumption when biased from 0.5 V power supply.

In contrast to these basic topologies based on common source transistor stages, there is a possibility to design such dual band capability with common gate stages as well. In this regard, a topology proposed in literature (Youssef & Haslett, 2007) uses a well-known architecture exploiting the current reuse, with two stacked NMOS and PMOS common gate transistors. Common gate topology is a must when dealing with wide bandwidth, this LNA prototype addressing the UWB standard. However, contrary to the wideband behavior at the input, the bands of interest (the UWB Groups 1 and 3) are selected at the output with the network shown in Fig. 3 *b*. The circuit, designed in a 0.18μm CMOS process, exhibits a maximum gain of 13.5 dB and minimum noise figure of 3.5 dB for 2.25 mW power consumption only.

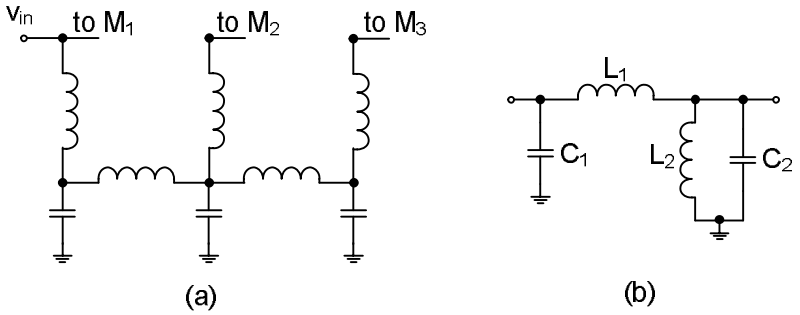

Fig. 3 – LC ladder used for positive feedback (*a*) and selective network for dual band capability (*b*).

An original solution, yet expensive if implemented with discrete components (Chen *et al*., 2015) but still feasible in CMOS implementation, consists of implementing two distinct LNAs, covering distinct standards, together with a Wilkinson power divider and another Wilkinson combiner, implemented on the same chip. The advantage of such implementation would be that each amplifier can be optimized particularly for one standard, therefore improving the transceiver performances.

3. Conclusions

Different design principles used to implement concurrent low noise amplifiers in CMOS technology were reviewed in this article. According to the previous work reported in the literature, much effort has been devoted to minimize the noise factor and increase the power gain, things not easy to deal with and even fulfil when taking into account the multi-standard capability. There is still work left to be carried out for implementing tri-band and even quad-band LNAs.

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IMPLEMENTĂRI DE AMPLIFICATOARE TIP LNA CU DUBLĂ ACOPERIRE ÎN FRECVENȚĂ ÎN TEHNOLOGIE CMOS

(Rezumat)

Cererea în creştere pentru transceivere multistandard în aplicațiile de comunicații mobile şi pentru terminalele portabile impune capabilitate multistandard şi

pentru amplificatoarele de tip LNA. Acest articol sintetizează cele mai importante tehnici utilizate la implementarea amplificatoarelor de tip LNA în tehnologie CMOS, duale, în concordanţă cu ceea ce s-a propus în literatură. Asemenea amplificatoare sunt suficiente pentru a viza un standard de comunicaţii mobile, de obicei cu două benzi de frecvenţe distincte alocate emiţătorului şi receptorului, două standarde distincte de comunicaţii wireless, precum WLAN (2.4 GHz şi 5 GHz), sau viza chiar o mixare a acestor două cazuri (o bandă pentru comunicaţii mobile – uplink sau downlink – şi un standard wireless). Aşa cum se poate constata, majoritatea acestor arhitecturi sunt implementate cu etaj de tip sursă comun, capabilitatea multistandard fiind implementată cu ajutorul unor celule rezonante LC (serie şi paralel). Din considerente de spaţiu, doar arhitecturile concurente sunt acoperite de acest articol.