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LOW-VOLTAGE CMOS-130 nm SUB-BANDGAP VOLTAGE REFERENCE

BY

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Abstract. A CMOS voltage reference operating at 1.2 V (± 10%) supply is presented. The circuit is designed in 130 nm CMOS technology and works in the temperature range [–20, +120] °C. The output reference voltage is 500 mV and adjustable up or down with tens of mV. The main performances of the circuit are the following: less than -60 dB power supply rejection rate, a line sensitivity of 0.37 mV/V, 3 ppm/ºC temperature coefficient and 0.4 nV/√Hz output squared noise at 1 Hz frequency. The current consumption does not exceed 6 µA in the worst case operating conditions.

Key words: sub-bandgap; low voltage; voltage reference; PVT sensitivities.

1. Introduction

Process variations, supply voltage and temperature (PVT) affect the operation of all electronic circuits. The output voltage of a reference circuit must have a constant value, which means a very low sensitivity to PVT variations.

Regarding temperature, two intrinsic characteristics of the bipolar junction are used in designing reference circuits: i) the emitter-base voltage decreases linearly with temperature, and ii) the difference of two emitter-base

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voltages (coming from two bipolar junctions with different current densities) increases linearly with temperature. Both voltage types are weakly sensitive to process variations.

Note that the threshold voltage of a MOS transistor also decreases linearly with temperature but it is very sensitive to process variations. Instead, the difference of two gate-source voltages, corresponding to MOS transistors which are working in sub-threshold region, increases linearly with temperature and is weakly sensitive to process variations.

The influence of supply voltage variations on the reference voltage can be greatly reduced by choosing an appropriate circuit schematic. To some extent, the circuit topology can also mitigate the influence of device mismatches and process variations.

Compared to a circuit supplied with voltages above 1.8 V, a low-voltage design (*i.e.*, supply voltage of 1.2 V or less) implies more restrictions in conceiving the architecture. In the case of reference circuits one may overcome some difficulties by using polysilicon resistors. But this leads to a greater influence of process variations because the technological corners of resistors and transistors are not correlated.

Although the concept of summing currents with positive and negative temperature coefficients underlies many proposed reference circuits, the implementations may be very different. The voltage reference with curvature correction presented in (Basyurt *et al.*, 2012) contains a simple feedback amplifier. Resistive voltage dividers and an OTA structure without a tail current source are used in (Wadhwa, 2008). Resistive dividers are also used in (Ker *et al.*, 2004). Other circuits include one symmetric OTA, by reason of low offset (Xing *et al.*, 2007) or two operational amplifiers (Chen *et al.*, 2014).

The circuit described in (Xu *et al.*, 2013) is not based on summing currents with opposite temperature coefficients; the reference voltage is equal to the extrapolated threshold voltage of a MOS transistor at 0 K.

The circuit presented in the next section contains only transistors and is based on summing voltages with positive and negative temperature coefficients.

2. Circuit Description

The schematic of the proposed low-voltage reference circuit is shown in Fig. 1. All MOS transistors are 1.2 V standard threshold voltage devices except for the differential pair of the amplifier named “amp1”, which are 1.2 V low threshold voltage devices. The capacitor *C* connected to the output node is made of NMOS transistors. Q_1 and Q_2 are vertical pnp bipolar transistors.

The circuit contains a start-up, two self-biased current generators and an output stage. The notations I_{ptc} and I_{ntc} refer to currents with positive and negative temperature coefficients. MOS transistors from inside I_{ptc} generator are sized so that Q_1, Q_2, M_1 and M_2 are crossed by the same current denoted by letter *I*, as shown in Fig. 1. The ratios of Q_1, Q_2 and M_1, M_2 are *N* and 4, respectively.

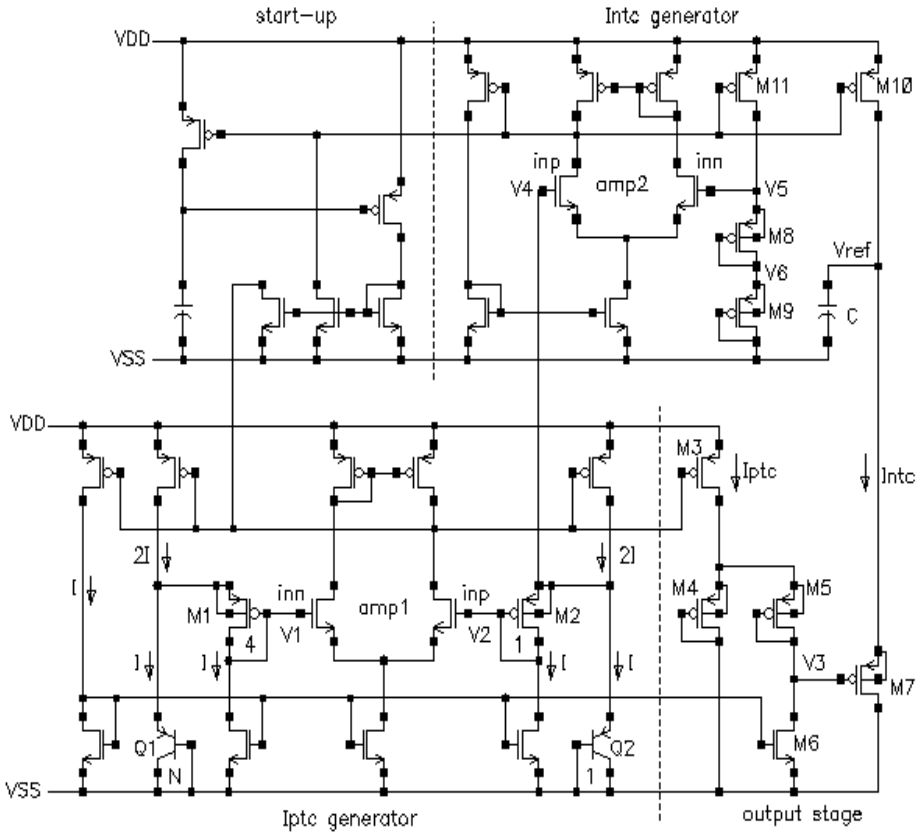

Fig. 1 – Schematic of proposed voltage reference circuit.

The amplifier "amp1" maintains equal, the input voltages V_1 and V_2 equal, so it follows that

$$V_{EB1} - V_{SG1} = V_{EB2} - V_{SG2}, \text{ or } V_{SG2} - V_{SG1} = V_T \ln N , \quad (1)$$

where: V_T is the thermal voltage. This equation is similar to that obtained in (Imbrea *et al.*, 2011; Imbrea, 2015) by using serial connections of PMOS and bipolar diodes. Here, diodes M_1 and M_2 are connected in parallel with Q_1 and Q_2, respectively, due to lower supply voltage.

The current I has a positive temperature coefficient. By proper sizing of M_1, M_2 and N, we may get a current increasing almost linearly with temperature, as demonstrated in (Imbrea, 2015)

$$I \approx C_1 T - C_2 , \quad (2)$$

where: T is the absolute temperature and C_1, C_2 are positive constants which depend on the transistor shapes, temperature coefficients of the threshold and gate-source voltages, and others.

The diagrams in Fig. 2, captured from a DC simulation, illustrate the biasing of the transistors M_1, M_2 and the current I produced by the I_{ptc} generator; V_{thp0} is the threshold voltage of M_1 and M_2 with sources connected to the bulk. While the temperature increases from –20ºC to +120ºC, M_2 goes from moderate to strong inversion and M_1 operates in weak inversion, tending to enter moderate inversion.

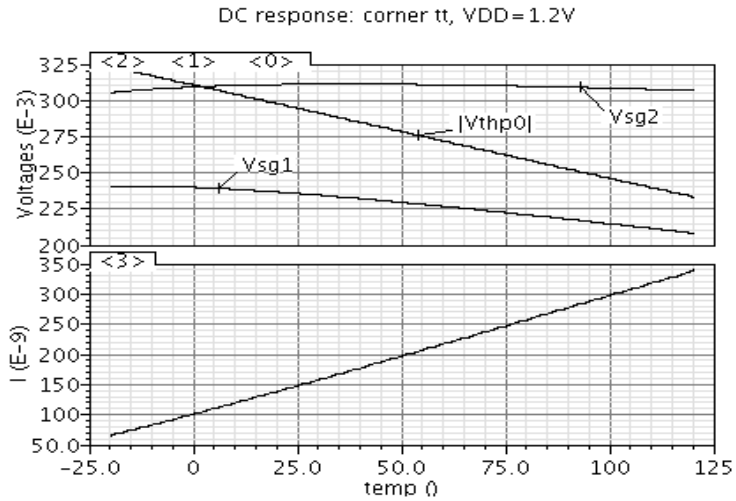

Fig. 2 – Biasing of M_1, M_2 and current I *vs.* temperature.

The linear dependence on temperature is not a necessary condition for the current I. The purpose is to obtain a voltage V_3 proportional to thermal voltage:

$$V_3 = V_{SG4} - V_{SG5} = C_3(V_{SG2} - V_{SG1}), \tag{3}$$

where: C_3 is a constant. This implies that the current through M_3 must be higher than the current through M_6 (both currents I_3 and I_6 are proportional to I).

The amplifier "amp2" maintains the input voltages V_4 and V_5 equal, so it follows that:

$$V_{EB2} = V_{SG8} + V_{SG9}. \tag{4}$$

If the transistors M_7, M_8 and M_9 have the same width/length and the currents flowing through M_{10} and M_{11} are equal, then:

$$V_{SG7} = V_{SG8} = V_{SG9} = \frac{V_{EB2}}{2}. \tag{5}$$

It is assumed that the channels of M_7, M_8 and M_9 are long enough to neglect the channel length modulation. One may see from (5) that I_{ntc} generator acts as a voltage divider. The output voltage can be calculated as follows:

$$V_{\text{ref}} = V_3 + V_{SG7} = C_3 V_{\text{T}} \ln N + \frac{1}{2} V_{EB2}. \tag{6}$$

The value of constant C_3 results from the condition $\partial V_{\text{ref}} / \partial T = 0$, knowing that $\partial V_{EB} / \partial T \simeq -2$ mV/ºC and $\partial V_{\text{T}} / \partial T \simeq +0.086$ mV/ºC. It helps sizing the transistors in the output stage.

$$C_3 = -\frac{1}{2 \ln N} \cdot \frac{\partial V_{EB2} / \partial T}{\partial V_{\text{T}} / \partial T} \tag{7}$$

Some corrections should be applied to the currents I_{ptc} and I_{ntc} in order to get a reference voltage almost constant over a wide range of temperature.

3. Simulation Results

The two voltages summed in the output stage and the resulting reference voltage (V_3, V_{SG7} and V_{ref}) are illustrated in Fig. 3.

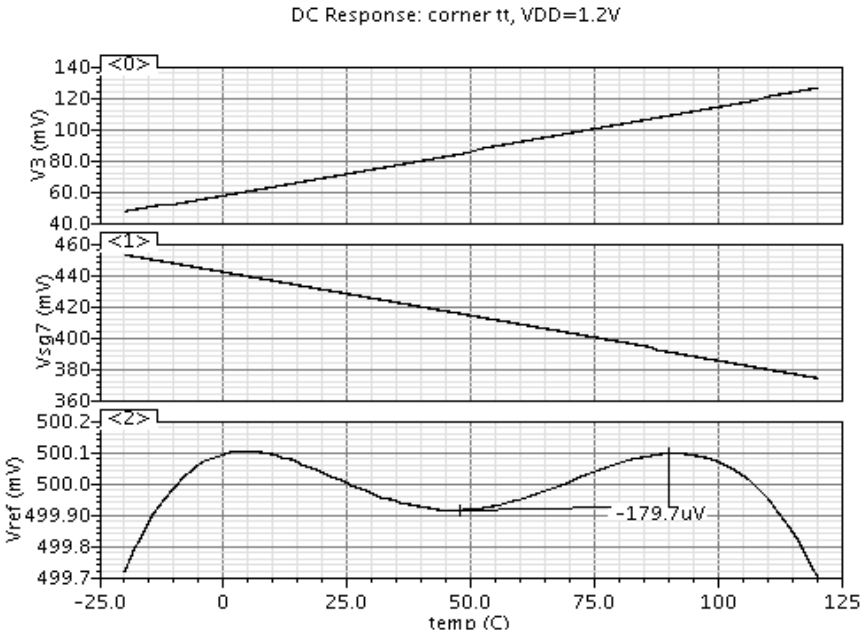

Fig. 3 – Temperature dependence of V_3, V_{SG7} and V_{ref}.

The temperature coefficient of V_{ref} is 2.8 ppm/ºC in the range [–13, 112]ºC. Voltages V_3 and V_{SG7} can be adjusted via the currents I_{ptc} and I_{ntc} so it is possible to obtain other values of V_{ref}. Another way is to adjust the width/length ratio of M_4 and M_5. Varying up or down V_3 without changing its slope is the easiest solution.

The influence of the supply line on the output voltage at DC or low frequencies is shown in Fig. 4. The output voltage changes by less than 90 µV while the supply voltage changes by ± 10%. This means a line sensitivity of 0.37 mV/V or 0.074 %/V.

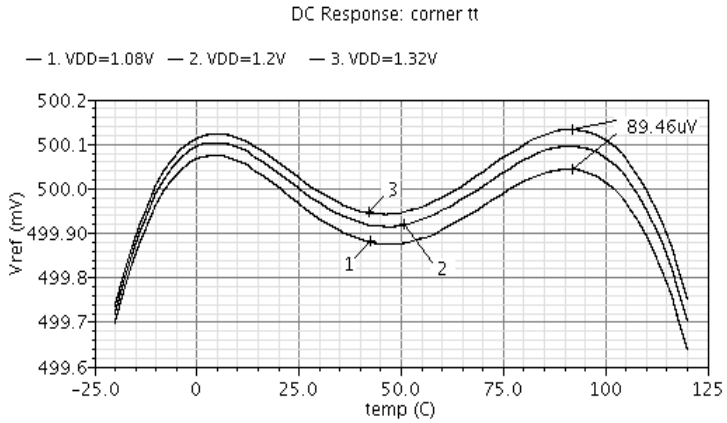

Fig. 4 – Line sensitivity of V_{ref}.

The line sensitivity is determined by the power supply rejection ratio (PSRR) at low frequencies. PSRR of the circuit is shown in Fig. 5. Capacitor *C*, with the value of 1 pF connected to the output node improves PSRR at high frequencies.

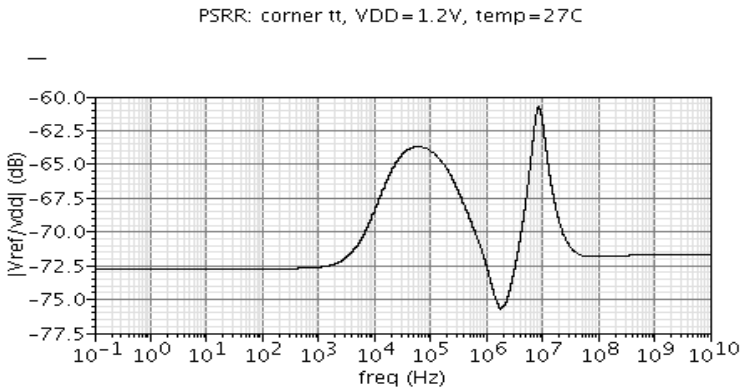

Fig. 5 – PSRR.

The transient response of the circuit to some supply voltage drops is shown in Fig. 6. There are no oscillations or overshoots. It means that the two differential amplifiers “amp1” and “amp2” are stable (the phase margin is greater than 60º).

The proposed circuit has also good noise characteristics, as can be seen in Fig. 7. The squared output noise at 1 Hz frequency is quite small,

approximately 0.4 nV/√Hz. The output capacitor *C* has almost no influence on the noise.

The process corners have a greater influence on V_{ref}, as shown in Fig. 8.

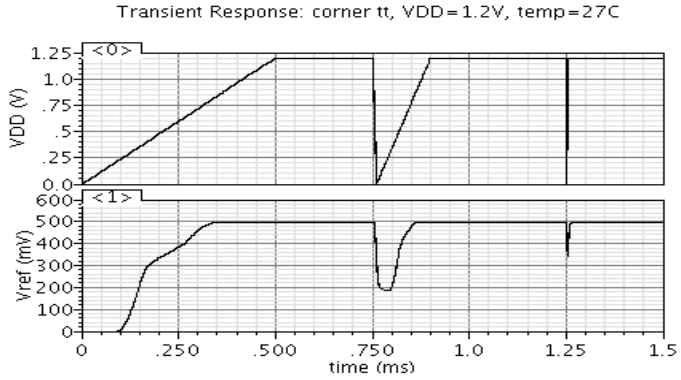

Fig. 6 – Start-up effectiveness.

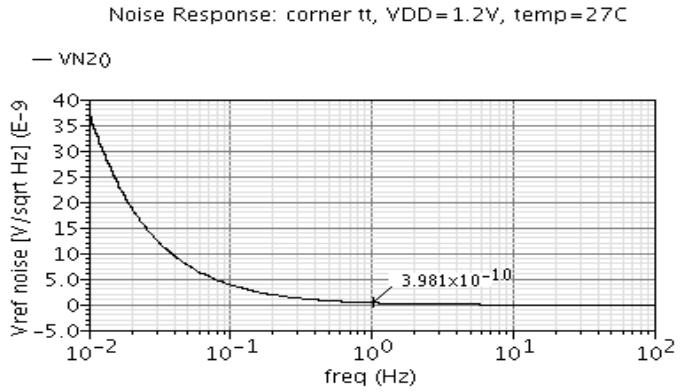

Fig. 7 – Squared output noise.

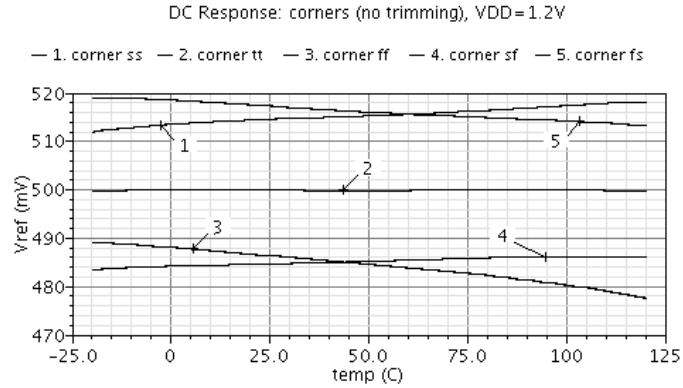

Fig. 8 – Influence of process corners on the reference voltage.

There are solutions to compensate for process variations. By adjusting the size of some transistors, we can modify the value or slope for one or both voltages V_3 and V_{SG7}. The results, after trimming only for slow-slow and fast-fast corners, are presented in Fig. 9.

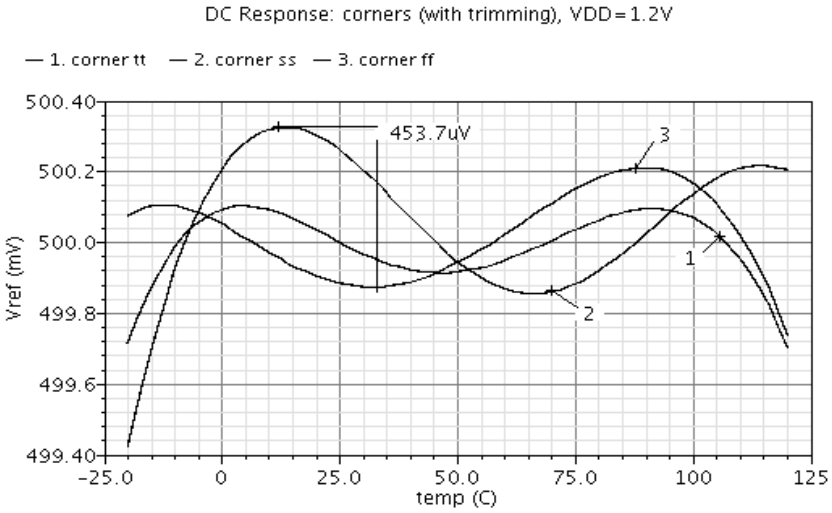

Fig. 9 – Compensation for process variations.

Current consumptions of the proposed circuit are shown in Fig. 10. In the worst case conditions (corner fast-fast and 1.32 V supply) the current does not exceed 6 µA. This means less than 8 µW power dissipation.

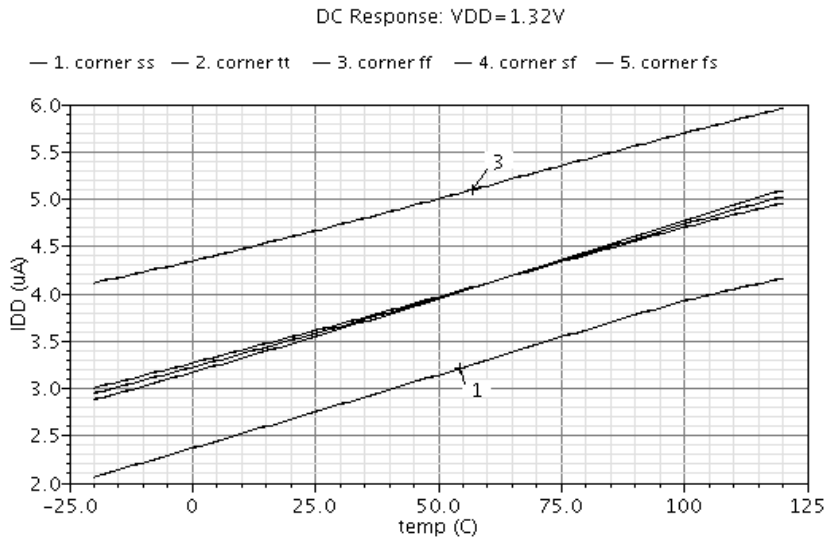

Fig. 10 – Current consumption.

4. Comparisons with Similar Works

Comparisons between this work and some referred to in this paper are listed in the Table 1. The performances of the voltage reference described here are comparable or superior to those shown in the table.

Table 1
Comparisons

	This work	Chen *et al*., 2014	Xu *et al*., 2013	Wadhwa, 2008	Xing *et al*., 2007
CMOS process	130 nm	350 nm	180 nm	90 nm	180 nm
Supply voltage	1.2 V	1.8 V	> 1.2 V	1.2 V	1.2 V
Reference voltage	500 mV	596 mV	620 mV	611 mV	657 mV
Line sensitivity	0.37 mV/V	0.74 mV/V	0.2 mV/V	7.5 mV/V	1.6 mV/V
Temperature coefficient	3 ppm/ºC	4 ppm/ºC	12.9 ppm/ºC	13.9 ppm/ºC	10 ppm/ºC
Temperature range	[–20, +120] ºC	[–60, +130] ºC	[–20, +80] ºC	[–40, +125] ºC	[0, +150] ºC
Power dissipation	< 8 µW	360 µW	0.21 µW	–	47 µW
PSRR @100Hz	–72.5 dB	–59 dB	–68 dB	–45 dB	–55 dB
Resistors	not used	used	not used	used	used

5. Conclusions

The low-voltage reference circuit described in this work is designed in 130 nm CMOS process by using only MOS transistors and vertical substrate PNP transistors; no on-chip resistors are used. Simulations show that the output voltage is weakly sensitive to temperature and supply voltage variations. The influence of process is greater but it can be compensated by adjusting the sizes of some transistors.

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REFERINȚĂ DE TENSIUNE CMOS-130 nm LOW-VOLTAGE

(Rezumat)

Se prezintă un circuit de tip referință de tensiune care funcționează cu tensiunea de alimentare 1.2 V (±10 %) în domeniul de temperatură [–20º, +120] ºC. Circuitul este proiectat într-o tehnologie CMOS-130 nm şi conține numai tranzistoare.

Tensiunea de ieşire are valoarea 500 mV în cornerul tipic şi poate fi modificată cu aproximativ ±10 mV prin ajustarea dimensiunilor unor tranzistoare. Variațiile tensiunii de alimentare şi a temperaturii au influențe relativ mici asupra tensiunii de referință (PSRR mai mare de 60 dB, sensibilitate 0.37 mV/V, coeficient de temperatură 3 ppm/ºC). Variațiile procesului tehnologic afectează într-o măsură mai mare tensiunea de referință însă există posibilități de compensare.

Curentul consumat de la sursa de alimentare nu depăşeşte valoarea de 6 μA în cornerul fast-fast şi 1.32 V tensiune de alimentare.