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A CIRCUIT SOLUTION FOR THE CONVERSION OF A GROUNDED CAPACITOR TO A FLOATING CAPACITOR

BY

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Abstract. A new solution for converting a grounded to floating capacitor is proposed. The circuit uses two negative feedback loops and a replica structure to obtain the intended behavior. The first feedback loop is responsible for the translation of the input voltage to the base grounded capacitor and the second for the translation of the capacitor current to the input terminal. The other terminal receives a replica of the base capacitor current with opposite sense. Capacitance multiplication can be achieved using the proposed circuit.

Key words: capacitance multiplication; floating capacitor; grounded capacitor.

1. Introduction

The capacitance dependence of a capacitor implemented with a MOS transistor of the DC voltage across it (Razavi, 2001) is well known. Regardless of whether we are talking about an NMOS or PMOS implementation, when the voltage across capacitor approaches 0, the equivalent capacitance of the structure drops to ~30% of the value corresponding to an appropriate biasing, as shown in Fig. 1.

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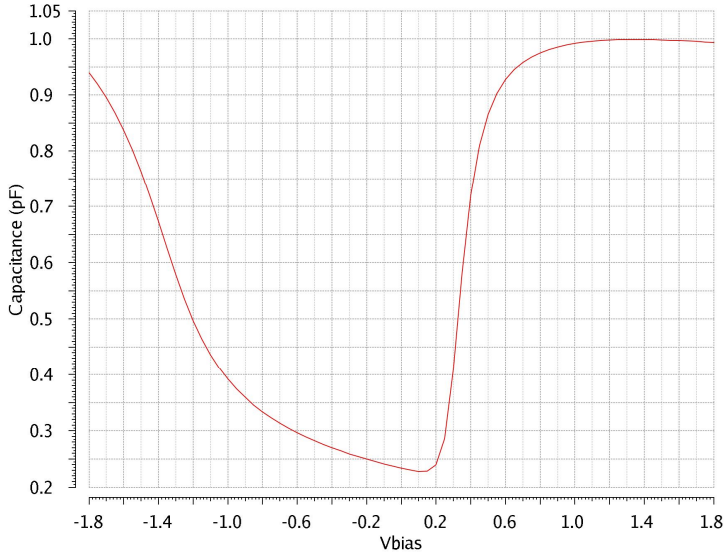

Fig. 1 – N-MOS equivalent capacitance versus the DC voltage across.

Many low frequency analog circuits use high value coupling capacitors and usually the CMOS technologies offer options for floating capacitors, but often these solutions come along with disadvantages: either huge area consumption or these devices alter the performance of the nearby ones, as is the case with poly-poly sandwich capacitor (Pennisi, 2002). This way the analog circuit designers feel the need for a circuit to convert the grounded capacitor to the floating capacitor. To this the need to have an analog/digital controlled multiplied capacitor, useful in a multitude of applications is added.

Usually a floating capacitor is used in order to multiply the capacitance (Chen *et al*., 2009; Solis-Bustos *et al*., 2000), but this way the capacitance of the base capacitor is reduced and the die area is high due to the fact that the N-MOS in a floating implementation needs a dedicated well and a dedicated substrate contact. There is a number of papers that study the multiplication of a grounded capacitor. The flipped voltage follower architecture is used in (Pennisi, 2002). but a floating equivalent capacitor is not available. The same flipped voltage follower technique is used in (Brînzoi *et al*., 2011) but the equivalent floating capacitor is based on an existing floating one. A very sophisticated implementation is presented in (Somdunyakanok *et al*., 2015) but here the multiplication factor is the square root of the two bias currents ratio, and that is limiting the multiplication range.

2. The Proposed Solution

The proposed circuit is based on the impedance control using a current scaling technique, as presented in Fig 2, negative feedback principle and also on replica circuit principle.

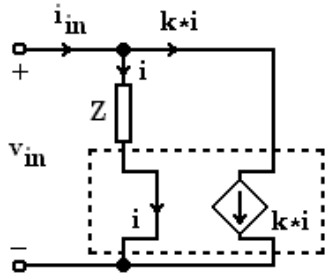

Fig. 2 – Current scaling principle.

The original solution that is able to convert the grounded capacitor to a floating one is presented in Fig. 3.

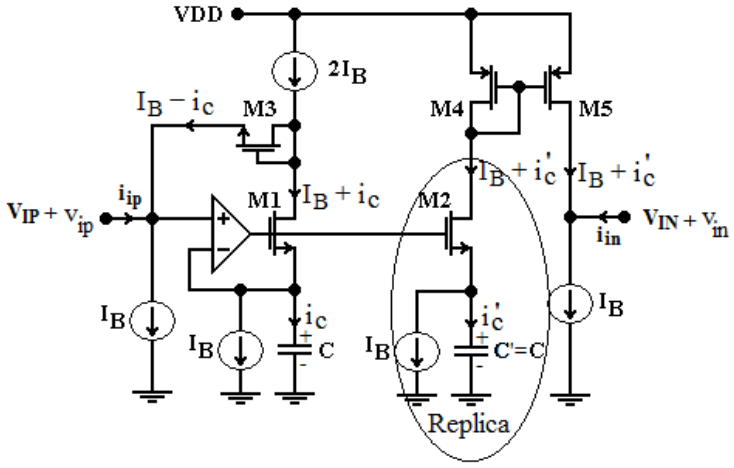

Fig. 3 – Proposed circuit for converting a grounded N-MOS capacitor to a floating capacitor

The negative feedback loop that includes the operational amplifier and the M_1 transistor minimizes the amplifier's differential input voltage. Consequently, the left input voltage and the voltage across the base capacitor *C* are going to be equal.

$$v_{ip} = v_c.$$

The M_1 transistor is biased by the I_B current source. The $i_c = v_{ip}/sC$ current is going to flow through M_1:

$$i_{M_1} = I_B + i_c .$$

The drain current of the M_1 transistor is:

$$i_{M_1} = 2I_B + i_{M_3}.$$

The negative feedback loop that includes the operational amplifier and the M_1, M_3 transistors makes the DC current through M_3 to be equal to I_B and consequently the signal current that flows into the left input of the block to be equal to the current through the base capacitor:

$$i_{ip} = i_c.$$

The M_3 transistor is necessary here in order to have an active region biasing for M_1.

The M2 transistor is a replica of M_1, being connected with the gate at the same potential as the gate of M_1, being biased using an identical current source I_B and having in source a capacitor C' equal to C. Consequently the signal current through M_2 will be:

$$i_c^{'} = i_c.$$

This current is mirrored to the right branch using the M_4–M_5 PMOS mirror. This way the right output current is going to be equal to the left input one and both of them are equal to the base capacitor current.

$$i_{ip} = i_c = i_c^{'} = -i_{in}.$$

The equivalent input impedance will be:

$$Z_{in} = \frac{(v_{ip} - v_{in})}{i_{ip}} = \frac{1}{sC}.$$

So the circuit behaves like a capacitor between the left and right terminals:

$$C_{eq} = C.$$

A complementary structure can be used in order to convert a P-MOS base capacitor to a floating capacitor, as Fig. 4 shows.

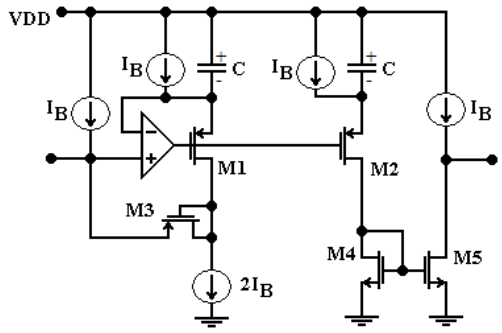

Fig. 4 – Proposed circuit for converting grounded P-MOS capacitor to a floating capacitor.

The amplifier used in the Fig. 3 circuit is a simple PMOS differential pair input folded cascode OTA architecture.

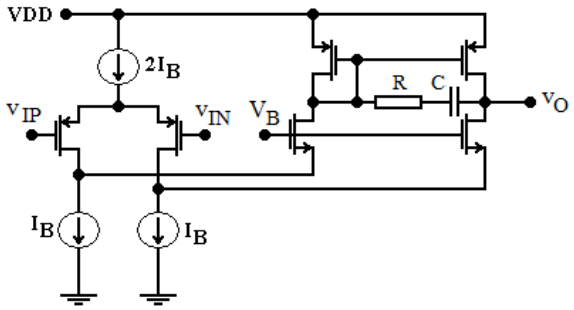

Fig. 5 – Circuit used as amplifier in the solution proposed in Fig. 3.

For the circuit that could be used in order to convert a P-MOS grounded capacitor a complementary structure will be used, with N-MOS differential input pair followed by a folded cascode.

A small signal analysis of the proposed circuit can be done using the following equivalent schematic.

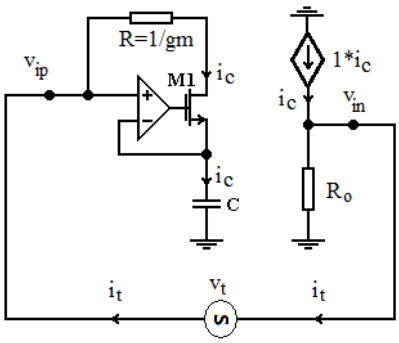

Fig. 6 – Small signal equivalent circuit for the solution proposed in Fig. 3.

Using this equivalent circuit one can write:

$$R_0(i_t - i_c) - v_t + v_{ip} = 0.$$

Due to the Amplifier – M_1 transistor negative feedback loop:

$$v_{ip} = v_c.$$

Due to the Amplifier – M_1 – R negative feedback loop:

$$i_t = i_c.$$

Finally:

$$\frac{v_t}{i_t} = \frac{v_c}{i_c} = \frac{1}{sC}.$$

Regarding the DC voltage range, the left amplifier input could go as low as a MOS transistor saturation voltage and must have a $V_{GS3}+V_{SAT}$ margin to the supply. The other terminal of the equivalent capacitor must have a V_{SAT} margin to both rails.

The maximum DC voltage across this capacitor will be:

$$V_{DC_{MAX}} = (V_{DD} - V_{SAT} - V_{GS}) - V_{SAT}.$$

The minimum DC voltage across this capacitor will be:

$$V_{DC_{MIN}} = V_{SAT} - (V_{DD} - V_{SAT}).$$

So, the operational DC range for this equivalent capacitor will be:

$$V_{DC} \in \left[-(V_{DD} - 2V_{SAT}); +(V_{DD} - 2V_{SAT} - V_{GS})\right].$$

The minimum supply voltage is given by a GS voltage and two saturation voltages of a MOS transistor, making it suitable for low voltage applications. In Brînzoi *et al.*, (2011), the minimum supply is given by two GS voltages and two saturation voltages.

$$V_{DD_{MIN}} = V_{GS} + 2V_{SAT}.$$

The same core circuit from Fig. 3 may be used also for capacitance multiplication, as shown in Fig. 7.

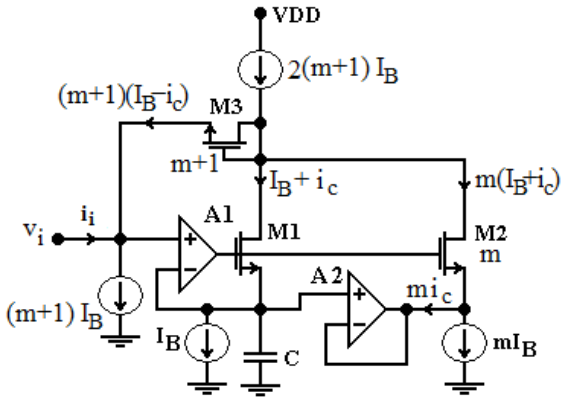

Fig. 7 – Proposed circuit for capacitance multiplication.

In this circuit an additional negative feedback loop around A2 amplifier equals the G-S voltages of M_1 and M_2. This way the current through M_2 will be m times higher than the one through M_1 in both DC and AC components.

$$i_{M_2} = m i_{M_1}.$$

The drain current of M_3 is:

$$i_{M_3} = 2(m+1)I_B - (m+1)(I_B + i_c).$$

The $(m + 1)(I_B - i_c)$ current is fed back to the input of the circuit where the DC component is subtracted. This way the current that will flow into the circuit becomes:

$$i_i = (m + 1)i_c.$$

The equivalent impedance at the input of the circuit will be:

$$Z_i = \frac{v_i}{i_i} = \frac{1}{s(m+1)C}.$$

This way, the Fig. 7 circuit behaves as a grounded capacitance multiplier by a (m + 1) factor:

$$C_{eq} = (m + 1)C.$$

The A2 amplifier used in the circuit from Fig. 7 has a very simple architecture, a simple PMOS differential pair input ota structure followed by a common source stage.

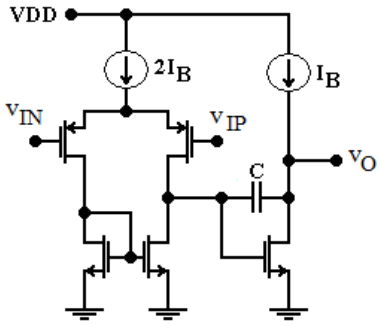

Fig. 8 – Circuit used as A2 amplifier in the solution proposed in Fig. 7.

Regarding the operational DC voltage range, the input could go as low as a MOS transistor saturation voltage and must have a $V_{GS} + V_{SAT}$ margin to the supply due to amplifiers needs.

$$V_{IN} \in [V_{SAT}; (V_{DD} - V_{SAT} - V_{GS})].$$

The minimum supply voltage requested by this capacitance multiplication circuit is the same as the one necessary for the Fig. 3 converter, making it suitable for low voltage applications.

By combining the structures from the Figs. 3 and 7, a grounded to floating capacitance multiplier can be obtained:

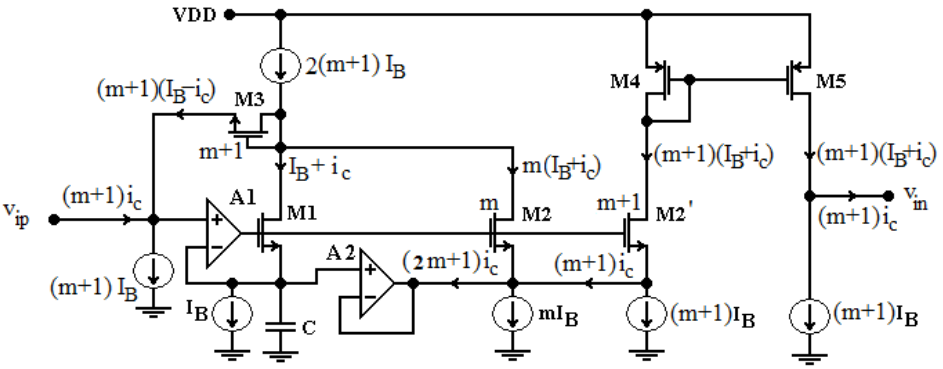

Fig. 9 – Circuit proposed for grounded to floating capacitance multiplier.

The equivalent input impedance for the structure proposed in Fig. 9 is:

$$Z_{in} = \frac{(v_{ip} - v_{in})}{i_{ip}} = \frac{1}{s(m+1)C}.$$

3. Simulation Results

The proposed circuit solutions were implemented at schematic level using the models of an AMS 0.18 um CMOS technology that uses a 1.8 V supply. Simulations were run using SPECTRE and there is a good agreement between the simulation results and the theoretical expectations.

Despite the fact that a much smaller base capacitor could be used in order to be converted/multiplied, the results further presented correspond to a grounded base capacitor of 10 pF due to the fact that an implementation that is using a smaller capacitor (*i.e.* 1 pF) makes no sense in terms of die areas. The difference between the area of two grounded capacitors and the one of a floating capacitor (if available) must cover the die area cost of the necessary circuits of the converter. The same observation is true for the difference between the equivalent (m + 1) multiplied capacitance and that of a (m + 1) capacitors directly instantiated from the library. The bias current used for amplifiers is 5 uA and the one used for converter/multiplier is 1 uA, making the solution appropriate for low power applications.

It must be mentioned that extra care was taken with the NFL1 (A1(out)–M_1–M_3–A1(+)) and NFL2 (A1(out)–M_1–A1(–)) negative feedback loops. In order to grant the stability of this loop, the A1 amplifier had to be frequency compensated.

The magnitude and phase response of the Fig. 3 circuit is plotted in Fig. 10. The capacitance behavior of the proposed structure is valid for 3 frequency decades.

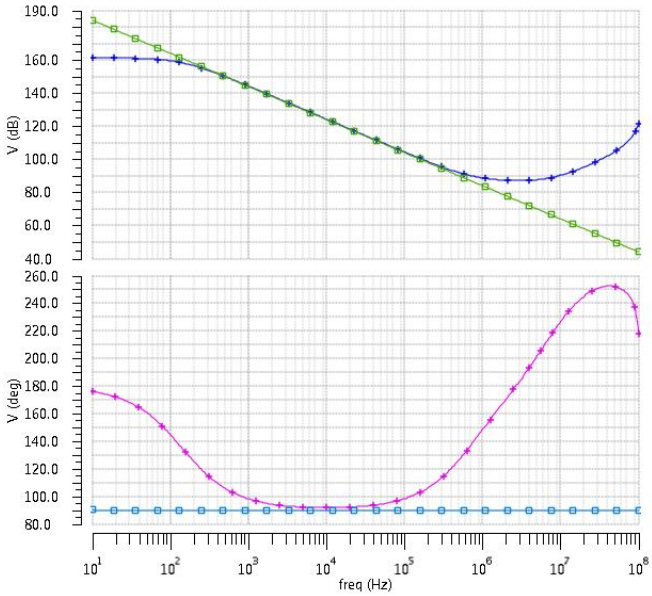

Fig. 10 – Magnitude and phase response of the grounded to floating converter, ideal (□) and real (+).

In Fig. 11 the magnitude and phase response of the proposed capacitance multiplier structure are plotted; the circuit is usable for 3 frequency decades. The response of the circuit proposed as grounded to floating capacitance multiplier is depicted in Fig. 12.

The next figure plots the THD of the input current evaluated at 1 kHz, 10 kHz and 100 kHz for different amplitudes of the voltage applied across the proposed converter.

The last figure plots the THD of the proposed capacitance multiplier's input current evaluated at 1 kHz, 10 kHz and 100 kHz for different amplitudes of the voltage applied at the input.

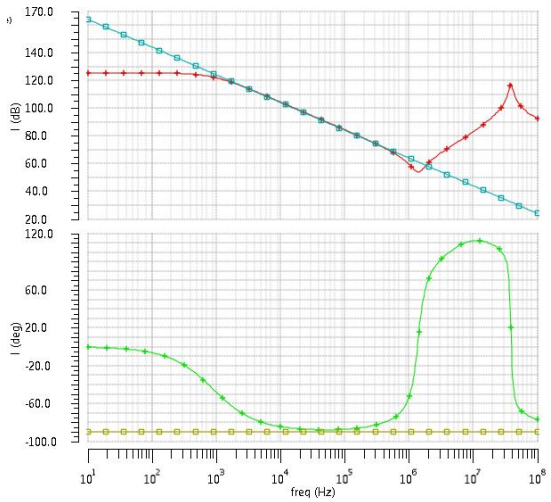

Fig. 11 – Magnitude and phase response of the capacitance multiplier, ideal (□) and real (+).

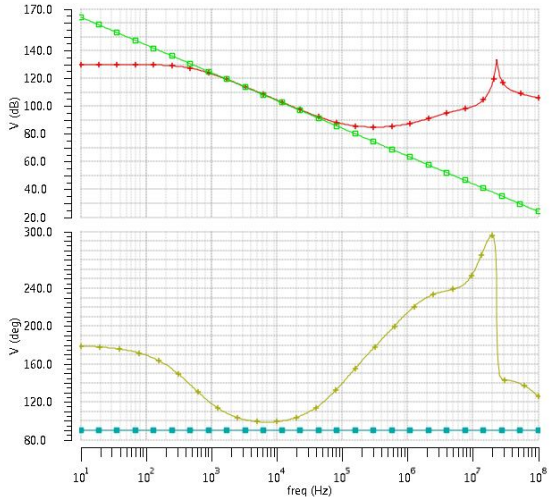

Fig. 12 – Magnitude and phase response of the grounded to floating capacitance multiplier, ideal (□) and real (+).

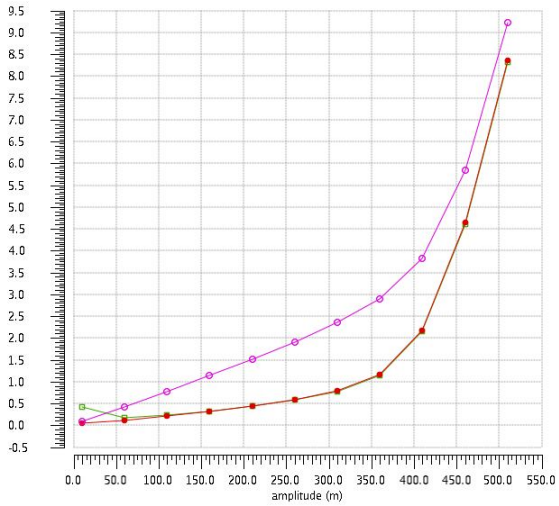

Fig. 13 – THD of the proposed converter input current versus input voltage amplitude for 1KHz (□), 10KHz (●) and 100KHz (○).

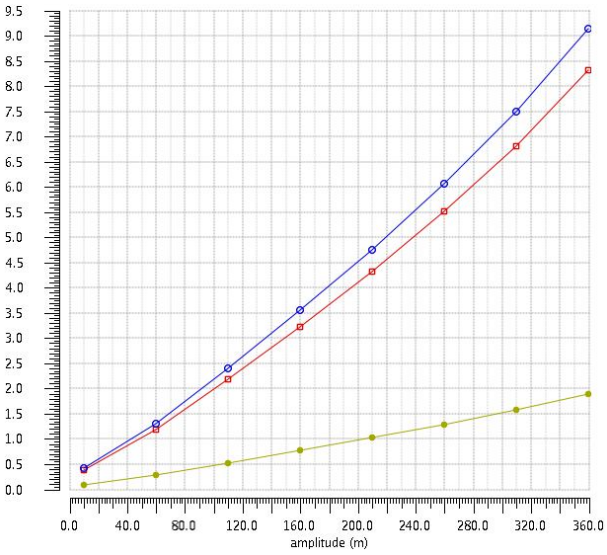

Fig. 14 – THD of the proposed capacitance multiplier's input current versus input voltage amplitude for 1KHz (□), 10KHz (●) and 100KHz (○).

4. Conclusions

An original structure that has the behavior of a floating capacitor starting from a base grounded one is presented. The capacitance multiplication is also possible. The equivalent capacitance is adjustable by activating-deactivating additional branches, so a digital control of the equivalent

capacitance can be done. Simulations results of a 0.18 um CMOS technology implementation agree well with the theoretical expectations.

REFERENCES

Brînzoi P., Crăcan A., Cojan N., *A New Approach in Designing Electrically Controlled Capacitance Multipliers*, Internat. Symp. on Signals, Circ. a. Syst. 2011, Iaşi, România.

Chen C.H., Mak P.I., Zhang T.T., Vai M.I., Mak P.U., Pun S.H., Wan F.,. Martins R.P., *A 2.4 Hz-to-10 kHz-Tunable Biopotential Filter using a Novel Capacitor Multiplier*, Prime Asia, 2009.

Pennisi S., *High Accuracy CMOS Capacitance Multiplier*, 9th Internat. Conf. Electron., Circ. a. Syst., 2002.

Razavi B., *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Internat. Edition, 2001.

Solís-Bustos S., Silva-Martínez J., Maloberti F., Sánchez-Sinencio E., *A 60-dB Dynamic-Range CMOS Sixth-Order 2.4-Hz Low-Pass Filter for Medical Applications*, IEEE Trans. on Circ. a. Syst., II: Analog and Digital Signal Proc., **47**, *12* (2000).

Somdunyakanok M., Angkeaw K., Prommee P., *Floating-Capacitance Multiplier Based on CCDDCCs and its Application*, IEEE Region 10 Annual Internat. Conf., Proc., 2015.

CIRCUIT DE CONVERSIE DE LA CONDESATOR CU UN TERMINAL LA MASĂ LA CONDENSATOR FLOTANT

(Rezumat)

Se propune un nou circuit de conversie de la condensator cu un terminal la masă la condensator flotant. Soluția de circuit utilizează două bucle de reacție negativă precum şi o structură replică pentru a obține comportamentul dorit. Cea dintâi este responsabilă pentru translarea tensiunii de intrare către condensatorul cu un terminal la masa de bază iar cea de-a doua de translarea la un terminal de intrare a curentului prin acest condensator. Celălalt terminal primeşte o replică a curentului prin condensatorul de bază dar cu sensul opus. Utilizând circuitul propus se poate obține şi multiplicarea capacitivă.