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ON THE USE OF CONTROLLED GAIN CURRENT MIRRORS IN THE IMPLEMENTATION OF TUNEABLE TRANSCONDUCTORS

BY

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Abstract. An extended discussion related to the use of the electrically controlled gain current mirrors in the implementation of the adjustable transconductors is proposed. Two previously presented solutions for the implementation of controlled gain mirrors are being studied in parallel and features like dynamic range, linearity or noise are reviewed. Both solutions are based on the behavior of two current controlled current amplifiers that use two unbalanced current mirror architectures.

Key words: current mirror; transconductor; OTA; tunable transconductance.

1. Introduction

In the modern information technology applications the opamp based active RC filters cannot fulfill specifications like wide bandwidth, low power and low voltage operation. The right approach is the use of the current mode circuit techniques in the design of the analog filters (Toumazou *et al.*, 1990). Given the fact that the analog sections of the chip must coexist near the digital processing ones and in order to minimize the die area the most successful

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approach is to use the operational transconductance amplifier to replace the operational voltage amplifier and the resistors in the active RC filters.

Given the fact that the G_m-C filters pole frequency depend on g_m/C, it follows that there are two solutions in adjusting the poles of the analog $G_m - C$ filter (Pavan *et al.*, 2002): the first one is to keep the G_m constant and to vary C, and the second to keep the C constant and to vary G_m. The evolution of the different filter parameters like mean squared noise, total necessary capacitance and total dissipated power versus the cutoff frequency of a programmable integrator is given in the Fig. 1.

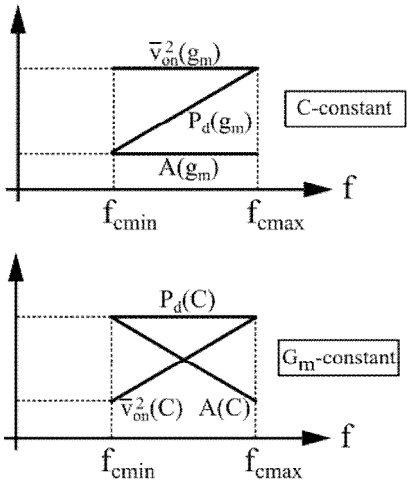


Fig. 1 – Variation of the filter parameters *versus* the cutoff frequency.

The limited resolution of the discrete control and the inherent non-ideal behavior of the switches are two important drawbacks of the discrete control, usually implemented by switching capacitors. It follows that in order to compensate the expected ±30% process variations of the integrated passive circuit elements, the only solution is the realization of some wide range tunable transconductors.

The use of the variable gain current mirrors in the implementation of the electrically controlled tunable transconductors is not a new idea. A tunable transconductor that uses a current mirror with triode operating transistors as degeneration is proposed on (Palmisano *et al.*, 2002), and although a ±50% mirror gain range is achievable, the current mirror gain depends on the control voltage by a nonlinear function.

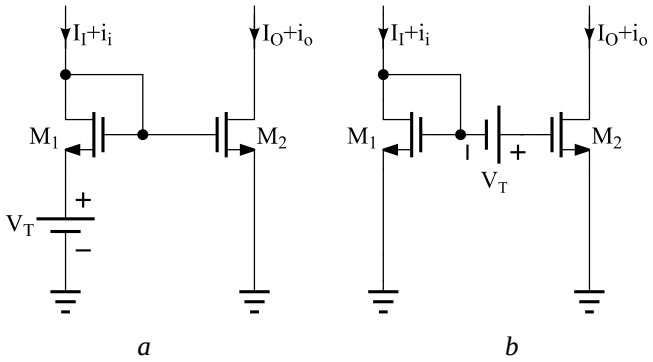
An adjustable transconductor comprised of a simple differential stage with source resistive degeneration used to convert the input differential voltage to a differential current which is fed to a current-controlled current amplifier implemented with an unbalanced current mirror that exhibits a wide tunable gain is presented in (Bonteanu *et al.*, 2017a) This circuit solution is

compared in this paper with the one proposed in (Bonteanu *et al.*, 2017b) where an improved transconductor whose operation is based on the behavior of an alternative unbalanced mirror architecture that will allow a superior performance for the filters in which it is used was presented.

2. Operation Principle

The basic principle is first explained using the simplified circuits shown in Fig. 1. On the V_{GS} loop of the Fig. 2, one can write in DC for both structures:

$$V_{GS2} = V_{GS1} + V_T. \tag{1}$$



a *b*

Fig. 2 – The simplified circuit of the unbalanced current mirror.

Using the square law for the MOS transistor, considering strong inversion for both devices and neglecting the body effect for the Fig. 2 *a* structure M_1 transistor, we can obtain:

$$\sqrt{\frac{I_O}{I_I}} = 1 + \sqrt{\frac{K}{I_I}} V_T, \tag{2}$$

where: I_O and I_I are the DC components of the output and input currents.

In the last relationship it is obvious that the DC gain becomes 1 if the tune voltage V_T is 0. Moreover, if I_I is a bias current, $I_I = I_B$, the output current is going to be a $\left(1+V_T\sqrt{K/I_B}\right)^2$ amplified version of that bias current.

One can write for small signal components:

$$i_o = g_{m2} v_{gs2}, \tag{3}$$

where: $g_m = 2\sqrt{KI_M}$ is the transconductance of the transistor and:

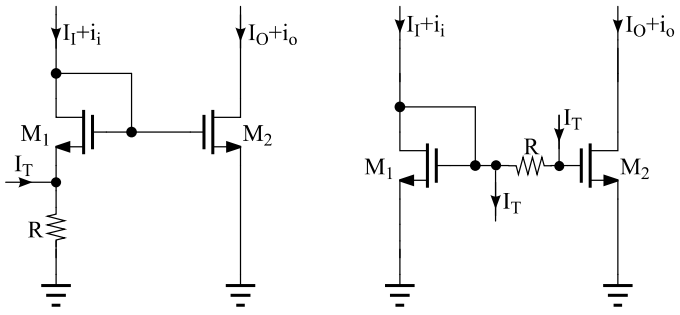
$$v_{gs2} = v_{gs1} = \frac{i_i}{g_{m1}}. \tag{4}$$

Using (2):

$$\frac{i_o}{i_i} = \frac{g_{m2}}{g_{m1}} = \sqrt{\frac{I_O}{I_I}} = 1 + \sqrt{\frac{K}{I_I}} V_T. \tag{5}$$

The last result show the voltage controlled current amplifier behavior of the Fig. 2 structures.

A practical way to implement the voltage sources of the Fig. 2 circuit is to use a resistor and a tune DC current, as Fig. 3 shows.



a *b*

Fig. 3 – Circuit implementation of the unbalanced current mirrors.

The DC relation between the currents of the structure from Fig. 3 *a*:

$$\sqrt{\frac{I_O}{I_I}} = 1 + R\sqrt{\frac{K}{I_I}}\left(I_T + I_I\right). \tag{6}$$

Considering that the input DC component is a constant bias current, $I_I = I_B$, the corresponding relationship between the small signal components will be:

$$a_i\left(I_T\right) = \frac{i_o}{i_i} = \frac{g_{m2}}{g_{m1}}\left(1 + g_{m1}R\right) = \left[1 + R\sqrt{\frac{K}{I_I}}\left(I_T + I_B\right)\right]\left(1 + 2\sqrt{KI_B}R\right). \tag{7}$$

Following the same steps for the Fig. 3b structure, we will get:

$$a_i\left(I_T\right) = \frac{i_o}{i_i} = 1 + R\sqrt{\frac{K}{I_B}} I_T. \tag{8}$$

The last result shows the current controlled current amplifier behavior of the unbalanced current mirror. The current gain is higher as I_T is higher and

I_B lower. The Fig. 3 *a* structure promises a larger gain compared to the Fig. 3 *b* one with a factor of $\left(1+2\sqrt{KI_B}R\right)$.

3. The Tunable Transconductor Implementation

In order to obtain a tunable transconductor, two cascoded instances of the previously presented unbalanced current mirrors are going to be used. A source resistive degenerated differential pair converts the differential input voltage to a differential input current that is fed to the input of the current amplifier. Two additional p type transistor cascoded current mirrors are used in order to complete the structure.

It must be mentioned an important difference between the Figs. 4 *a* and 4 *b* structures regarding the input voltage dynamic range: giving the fact that in Fig. 4 *b* circuit the tune resistor is no longer connected in series to the master of the current mirror used as current amplifier, the dynamic range at the input of this transconductor will be better.

Another important difference between the transconductor structures is related to the doubled count of tune current sources necessary for the Fig. 4 *b* structure compared to the Fig. 4 *b* one. This will lead to additional die area.

Considering the degenerative resistance large enough and R_{S1} = = R_{S2} = R_S, the input differential pair currents are going to be:

$$\begin{cases} i_{I1} = I_B + \dfrac{v_{ID}}{2R_S}, \\ i_{I2} = I_B - \dfrac{v_{ID}}{2R_S}. \end{cases} \tag{9}$$

Using the results of the unbalanced current mirror study, relation (8), on the M4-M6-M8 and M3-M5-M7 structures:

$$\begin{cases} i_{o1} = a_i\left(I_T\right)i_{i1} = +a_i\left(I_T\right)\dfrac{v_{id}}{2R_S}, \\ i_{o2} = a_i\left(I_T\right)i_{i2} = -a_i\left(I_T\right)\dfrac{v_{id}}{2R_S}. \end{cases} \tag{10}$$

The differential output current can be expressed as:

$$i_{o1} = \frac{i_{op} - i_{on}}{2} = i_{o1} - i_{o2} = a_i\left(I_T\right)\frac{v_{id}}{R_S}. \tag{11}$$

Consequently the transconductance can be written:

$$G_m = \frac{\partial i_{od}}{\partial v_{id}} = \frac{a_i\left(I_T\right)}{R_S}. \tag{12}$$

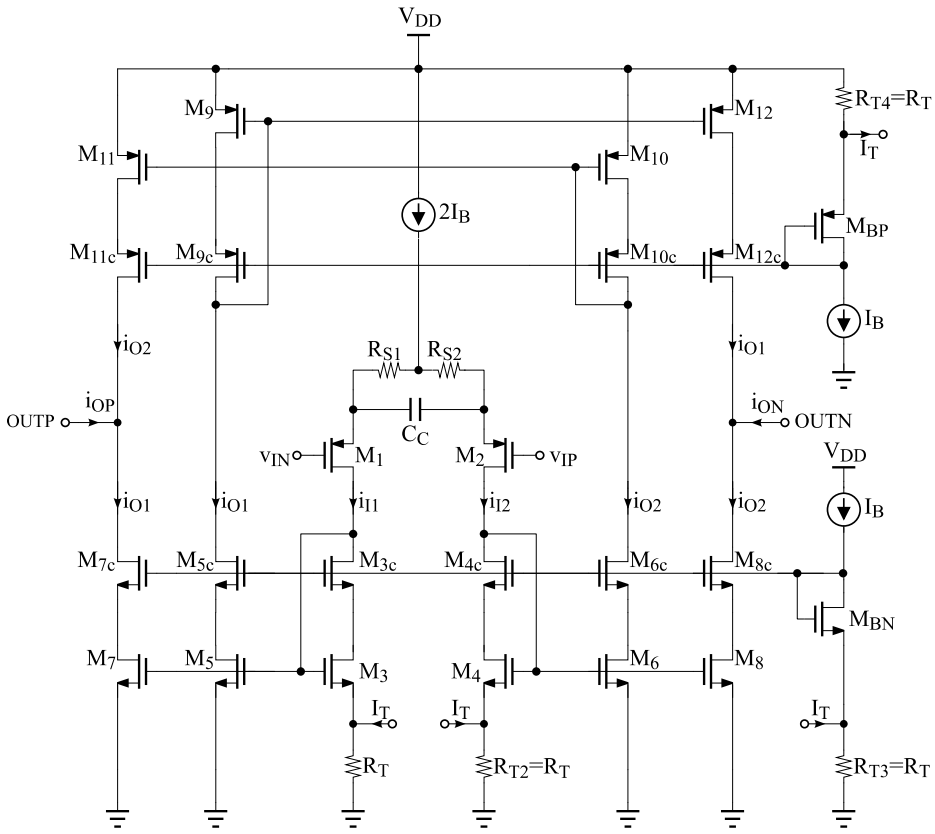


Fig. 4 *a* – Tunable transconductor implementation using Fig. 3 *a* structure.

Using (7), the transcondcutance of the Fig. 4a OTA will be:

$$G_m = \frac{1}{R_S}\left[1+\frac{g_{m3}R_T}{2}\left(3+\frac{I_T}{I_B}\right)+\frac{\left(g_{m3}R_T\right)^2}{2}\left(1+\frac{I_T}{I_B}\right)\right]. \tag{13}$$

Using Eq. (8), the transconductance of the Fig. 4 *b* OTA will be:

$$G_m = \frac{1}{R_S}\left(1+R_T\sqrt{\frac{K}{I_B}I_T}\right). \tag{14}$$

The last relationships show that the transconductance of the presented circuits is tunable by the I_T current. The Fig. 4 *a* structure promises a larger maximum transconductance compared to the Fig. 4 *b* one with a factor of $\left(1+2\sqrt{KI_B}R\right)$.

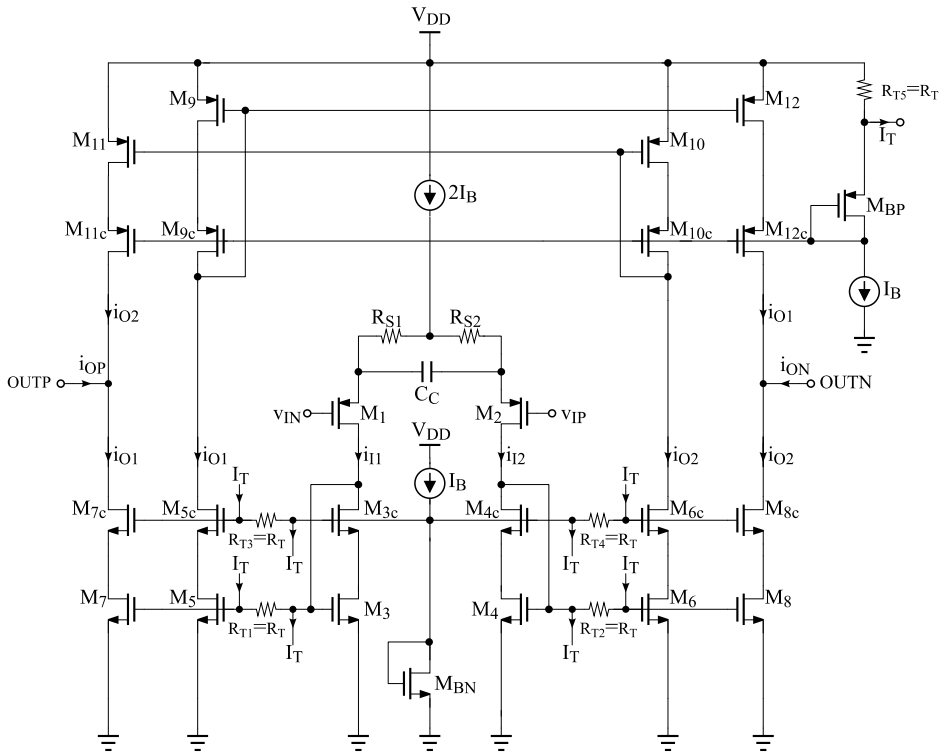


Fig. 4 *b* – Tunable transconductor implementation using Fig. 3 *b* structure.

4. Transconductor Frequency Analysis

The frequency analysis was performed using Fig. 5 simplified circuits, where C_C is the phase delay compensation capacitor used here in order to expand the bandwidth, C_G is the total capacitance in M_3 gate node and C_O is the output capacitance.

The transfer function expression will be:

$$H(s)=\frac{V_O(s)}{V_I(s)}=\frac{A_0\left(1+\dfrac{s}{z}\right)}{\left(1+\dfrac{s}{p_1}\right)\left(1+\dfrac{s}{p_2}\right)\left(1+\dfrac{s}{p_3}\right)}, \tag{15}$$

where:

$$z=\frac{1}{2C_C R_S}; \qquad p_1=\frac{1}{C_O R_o};$$
$$p_2=\frac{g_{m3}}{C_G\left(1+g_{mx}R_T\right)}; \quad p_3=\frac{1+g_{m1}R_S}{2C_C R_S}. \tag{16}$$

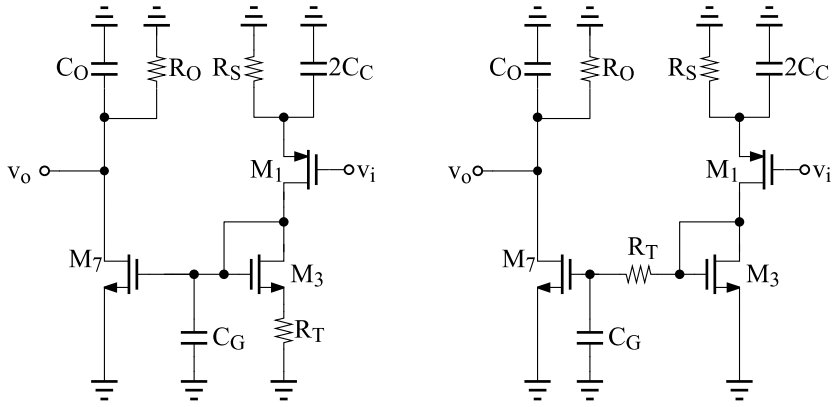


Fig. 5 –Simplified circuits for frequency analysis

The last relationship shows that both structures of the Fig. 4 have the same frequency behavior.

5. Transconductor Nonlinearity Analysis

For the nonlinearity analysis of the transconductor we used the square-law model for the MOS transistor and we considered that the input stage (M_1, M_2, R_{S1} and R_{S2}) is linear due to the degeneration resistors, so relations (9) are true.

For the Fig. 4 *b* structure, one can write on the M_5, M_3, R_{T1} loop:

$$v_{GS5} = v_{GS3} + R_T I_T, \tag{17}$$

which can be written as:

$$K\left(v_{GS5} - V_{TH}\right)^2 = K\left(v_{GS3} - V_{TH}\right)^2 + 2K\left(v_{GS3} - V_{TH}\right)R_T I_T + KR_T^2 I_T^2, \tag{18}$$

that is equivalent to:

$$i_{O1} = i_{I1} + 2\sqrt{K}\sqrt{i_{I1}}R_T I_T + KR_T^2 I_T^2. \tag{19}$$

A similar result is obtained for i_{O2}:

$$i_{O2} = i_{I2} + 2\sqrt{K}\sqrt{i_{I2}}R_T I_T + KR_T^2 I_T^2. \tag{20}$$

The differential output current will be:

$$i_{OD} = \frac{i_{O1} - i_{O2}}{2} = \frac{i_{I1} - i_{I2}}{2} + \sqrt{K}R_T I_T\left(\sqrt{i_{I1}} - \sqrt{i_{I2}}\right). \tag{21}$$

Using (9):

$$i_{OD} = \frac{v_{ID}}{2R_S} + \sqrt{K}R_T I_T\left(\sqrt{i_{I1}} - \sqrt{i_{I2}}\right). \tag{22}$$

Expanding $i_{OD}(v_{ID})$ in Taylor series up to the third term around $v_{ID} = 0$ we obtain an expression of the form:

$$i_{OD} = f\left(v_{ID}\right) = a_0 + a_1 v_{ID} + a_2 v_{ID}^2 + a_3 v_{ID}^3. \tag{23}$$

The first, second and third order derivatives of the (22):

$$\frac{\partial i_{OD}}{\partial v_{ID}} = \frac{1}{2R_S}\left[1 + \frac{\sqrt{k}R_T I_T}{2}\left(\frac{1}{\sqrt{i_{I1}}} + \frac{1}{\sqrt{i_{I2}}}\right)\right], \tag{24}$$

$$\frac{\partial^2 i_{OD}}{\partial v_{ID}^2} = \frac{\sqrt{k}R_T I_T}{16R_S^2}\left(-\frac{1}{\sqrt{i_{I1}^3}} + \frac{1}{\sqrt{i_{I2}^3}}\right), \tag{25}$$

$$\frac{\partial^3 i_{OD}}{\partial v_{ID}^3} = \frac{3\sqrt{k}R_T I_T}{64R_S^3}\left(\frac{1}{\sqrt{i_{I1}^5}} + \frac{1}{\sqrt{i_{I2}^5}}\right). \tag{26}$$

In order to write the Taylor series for $i_{OD}(v_{ID})$ up to the third power of v_{ID} we have to compute i_{OD}, $\partial i_{OD}/\partial v_{ID}$, $\partial^2 i_{OD}/\partial v_{ID}^2$ and $\partial^3 i_{OD}/\partial v_{ID}^3$ around $v_{ID} = 0$ when $i_{I1} = i_{I2} = I_B$:

$$a_0 = i_{OD}\big|_{v_{ID}=0} = 0, \tag{27}$$

$$a_1 = \left.\frac{\partial i_{OD}}{\partial v_{ID}}\right|_{v_{ID}=0} = \frac{1}{2R_S}\left(1 + \sqrt{k}R_T\frac{I_T}{\sqrt{I_B}}\right), \tag{28}$$

$$a_2 = \left.\frac{\partial^2 i_{OD}}{\partial v_{ID}^2}\right|_{v_{ID}=0} = 0, \tag{29}$$

$$a_3 = \left.\frac{\partial^3 i_{OD}}{\partial v_{ID}^3}\right|_{v_{ID}=0} = \frac{3\sqrt{k}R_T}{32R_S^3}\cdot\frac{I_T}{\sqrt{I_B^5}}. \tag{30}$$

Finally, we can write for the Fig. 4 *b* structure:

$$\mathrm{TDH} \approx \frac{1}{4}\left|\frac{a_3}{a_1}\right|V_{id}^2 = \frac{3\sqrt{k}R_T I_T}{64R_S^2 I_B^2\left(\sqrt{I_B} + \sqrt{k}R_T I_T\right)}V_{id}^2. \tag{31}$$

Following the same steps for Fig. 4 *a* structure we get:

$$\mathrm{TDH} \approx \frac{1}{4}\cdot\frac{g_{m3}R_T}{8R_S^3}\cdot\frac{3}{4}\cdot\frac{I_B - I_T}{I_B^3}\cdot\frac{R_S}{1+\frac{\left(g_{m3}R_T\right)^2}{2}\left(1+\frac{I_T}{I_B}\right)+\frac{g_{m3}R_T}{2}\left(3+\frac{I_T}{I_B}\right)}V_{id}^2. \quad (32)$$

Comparing the last relationships, it can be seen that the two structures exhibit similar linearity performance.

6. Transconductor Noise Analysis

The noise analysis was done for the Fig. 4 *b* structure on the Fig. 6 simplified differential half-circuit of the transconductor. The noise sources were considered uncorrelated. The i_{noh} noise current source is the noise coming from the other half of the differential half-circuit.

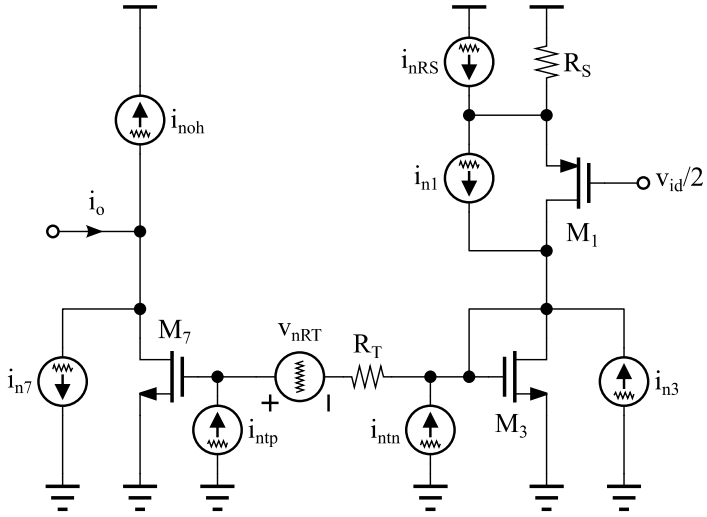


Fig. 6 –Differential half-circuit of the Fig. 4 *b* transconductor with added noise sources.

The resulting noise in the output can be written as:

$$\begin{aligned} i_{no} &= i_{noh} + i_{n7} + g_{m7}v_{nR_T} + \left(R_T + \frac{1}{g_{m3}}\right)g_{m7}i_{ntp} + \\ &+ \frac{g_{m7}}{g_{m3}}\left[i_{ntn} + i_{n3} + \left(\frac{g_{m1}R_S}{1+g_{m1}R_S}i_{nRS} + \frac{1}{1+g_{m1}R_S}i_{n1}\right)\right]. \end{aligned} \quad (33)$$

Thus the power spectral density (PSD) of the output noise current results as:

$$\overline{i_{no}^2}=\overline{i_{noh}^2}+\overline{i_{n7}^2}+g_{m7}^2\overline{v_{nR_T}^2}+\left(1+g_{m3}R_T\right)^2\left(\frac{g_{m7}}{g_{m3}}\right)^2\overline{i_{ntp}^2}+$$
$$+\left(\frac{g_{m7}}{g_{m3}}\right)^2\left[\overline{i_{ntn}^2}+\overline{i_{n3}^2}+\left(\frac{g_{m1}R_S}{1+g_{m1}R_S}\right)^2\overline{i_{nRS}^2}+\left(\frac{1}{1+g_{m1}R_S}\right)^2\overline{i_{n1}^2}\right]. \tag{34}$$

Due to the fact that the other half of the differential half-circuit has identical noise characteristics, we can substitute $\overline{i_{noh}^2}$ with the rest of the above expression, thus the output noise current PSD becomes

$$\overline{i_{no}^2}=2\left\{\overline{i_{n7}^2}+g_{m7}^2\overline{v_{nR_T}^2}+\left(1+g_{m3}R_T\right)^2\left(\frac{g_{m7}}{g_{m3}}\right)^2\overline{i_{ntp}^2}+\right.$$
$$\left.+\left(\frac{g_{m7}}{g_{m3}}\right)^2\left[\overline{i_{ntn}^2}+\overline{i_{n3}^2}+\left(\frac{g_{m1}R_S}{1+g_{m1}R_S}\right)^2\overline{i_{nRS}^2}+\left(\frac{1}{1+g_{m1}R_S}\right)^2\overline{i_{n1}^2}\right]\right\}. \tag{35}$$

In order to refer the output noise to the input of the transconductor one must divide the output noise current power spectral density by the square of the overall transconductance $g_m=\left[g_{m1}R_S/\left(1+g_{m1}R_S\right)\right]\left(g_{m7}/g_{m3}\right)$. Therefore the input noise voltage PSD can be written as:

$$\overline{v_{ni}^2}=2\left(\frac{1+g_{m1}R_S}{g_{m1}}\cdot\frac{g_{m3}}{g_{m7}}\right)^2\overline{i_{n7}^2}+\left(\frac{1+g_{m1}R_S}{g_{m1}}\right)^2g_{m7}^2\overline{v_{nR_T}^2}+$$
$$+2\left(\frac{1+g_{m1}R_S}{g_{m1}}\right)^2\left(1+g_{m3}R_T\right)^2\overline{i_{ntp}^2}+$$
$$+2\left(\frac{1+g_{m1}R_S}{g_{m1}}\right)^2\left(\overline{i_{ntn}^2}+\overline{i_{n3}^2}\right)^2+2R_S^2\overline{i_{nRS}^2}+2\left(\frac{1}{g_{m1}}\right)^2\overline{i_{n1}^2}. \tag{36}$$

Considering only thermal noise for the transistors the expression of the input noise voltage PSD becomes

$$\overline{v_{ni}^2}=2\cdot4kT\gamma\left\{\left(\frac{1+g_{m1}R_S}{g_{m1}}\right)^2\cdot\right.$$
$$\left.\cdot\left[\left(\frac{g_{m3}}{g_{m7}}\right)^2g_{m7}+\left(1+g_{m3}R_T\right)^2g_{mtp}+g_{m3}^2\frac{R_T}{\gamma}+g_{mtn}+g_{m3}\right]+\frac{R_S}{\gamma}+\frac{1}{g_{m1}}\right\}. \tag{37}$$

The noise analysis is done for the Fig. 4 *a* structure on the Fig. 7 simplified differential half-circuit of the transconductor.

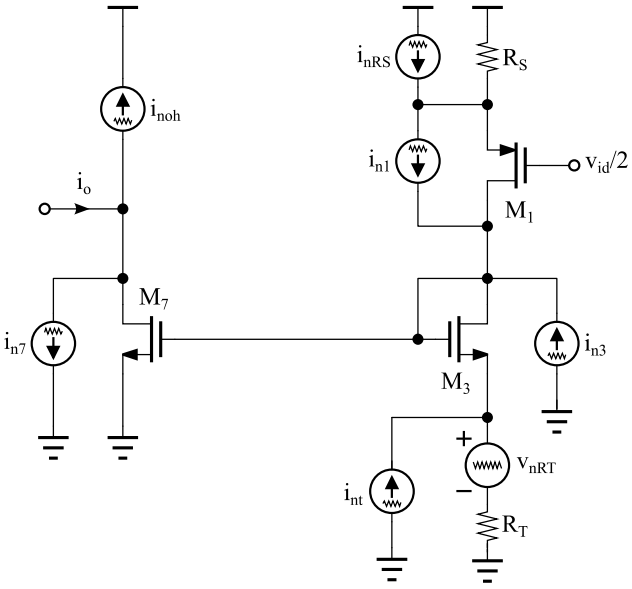


Fig. 7 –Differential half-circuit of the Fig. 4 *a* transconductor with added noise sources.

The resulting noise in the output can be written as:

$$i_{no} = i_{noh} + i_{n7} + g_{m7}\left(v_{nR_T} + i_{nt}R_T\right) + g_{m7}\left(\frac{1}{g_{m3}} + R_T\right)\times \\ \times\left[i_{n3} + \left(\frac{g_{m1}R_S}{1+g_{m1}R_S}i_{nR_S} + \frac{1}{1+g_{m1}R_S}i_{n1}\right)\right]. \tag{38}$$

Thus the power spectral density (PSD) of the output noise current results as:

$$\overline{i_{no}^2} = \overline{i_{noh}^2} + \overline{i_{n7}^2} + g_{m7}^2\left(\overline{v_{nR_T}^2} + \overline{i_{nt}^2}R_T^2\right) + g_{m7}^2\left(\frac{1}{g_{m3}} + R_T\right)^2 \times \\ \times\left[\overline{i_{n3}^2} + \left(\frac{g_{m1}R_S}{1+g_{m1}R_S}\right)^2\overline{i_{nR_S}^2} + \left(\frac{1}{1+g_{m1}R_S}\right)^2\overline{i_{n1}^2}\right]. \tag{39}$$

Due to the fact that the other half of the differential half-circuit has identical noise characteristics, we can substitute $\overline{i_{noh}^2}$ with the rest of the above expression, thus the output noise current PSD becomes

$$\overline{i_{no}^2} = 2\left\{\overline{i_{n7}^2} + g_{m7}^2\left(\overline{v_{nR_T}^2} + \overline{i_{nt}^2}R_T^2\right) + g_{m7}^2\left(\frac{1}{g_{m3}} + R_T\right)^2 \times \right.$$
$$\left. \times\left[\overline{i_{n3}^2} + \left(\frac{g_{m1}R_S}{1+g_{m1}R_S}\right)^2\overline{i_{nR_S}^2} + \left(\frac{1}{1+g_{m1}R_S}\right)^2\overline{i_{n1}^2}\right]\right\}. \quad (40)$$

In order to refer the output noise to the input of the transconductor one must divide the output noise current power spectral density by the square of the overall transconductance

$$g_m = \frac{g_{m7}g_{m1}}{1+g_{m1}R_S}\left(\frac{1}{g_{m3}} + R_T\right).$$

Therefore the input noise voltage PSD can be written as:

$$\overline{v_{ni}^2} = 2\left(\frac{1+g_{m1}R_S}{g_{m7}g_{m1}}\cdot\frac{g_{m3}}{1+g_{m3}R_T}\right)^2\left\{\overline{i_{n7}^2} + g_{m7}^2\left(\overline{v_{nR_T}^2} + \overline{i_{nt}^2}R_T^2\right) + g_{m7}^2\left(\frac{1}{g_{m3}} + R_T\right)^2 \times \right.$$
$$\left. \times\left[\overline{i_{n3}^2} + \left(\frac{g_{m1}R_S}{1+g_{m1}R_S}\right)^2\overline{i_{nRS}^2} + \left(\frac{1}{1+g_{m1}R_S}\right)^2\overline{i_{n1}^2}\right]\right\}. \quad (41)$$

Considering only thermal noise for the transistors the expression of the input noise voltage PSD becomes

$$\overline{v_{ni}^2} = 8kT\gamma\left(\frac{1+g_{m1}R_S}{g_{m7}g_{m1}}\cdot\frac{g_{m3}}{1+g_{m3}R_T}\right)^2\left\{g_{m7} + g_{m7}^2\left(\frac{R_T}{\gamma} + g_{mt}R_T^2\right) + \right.$$
$$\left. + g_{m7}^2\left(\frac{1}{g_{m3}} + R_T\right)^2\left[g_{m3} + \left(\frac{g_{m1}R_S}{1+g_{m1}R_S}\right)^2\frac{1}{\gamma R_S} + \left(\frac{1}{1+g_{m1}R_S}\right)^2 g_{m1}\right]\right\}. \quad (42)$$

The theoretical analysis reveals the fact that the input referred noise can be further lowered by decreasing the transconductance of the tuning current sources transistors. Comparing the (37) and (42) relationships, it is obvious that the Fig. 4 *a* structure performs much better concerning noise giving the fact that in the Fig. 4 *b* circuit the noise sources introduced by the tuning elements are in double count.

7. Conclusions

This paper presents a comparative analysis related to the use of the electrically controlled gain current mirrors in the implementation of the adjustable transconductors. Two previously presented solutions for the

implementation of controlled gain current mirrors were studied in parallel and features like input dynamic range, tuning range, frequency behavior, linearity and noise of the resulted tunable transconductors were reviewed. The results of this comparison, pros and cons for each solution, are summarized in Table 1.

Table 1
Compared Performances of the Tunable Transconductor Structures

	Fig. 4 *a* structure	Fig. 4 *b* structure
Die area	+	–
G_{m_max}	+	–
G_m tune range	+	–
Linearity	0	0
Input dynamic range	–	+
Noise	+	–
Frequency	0	0

REFERENCES

Bonteanu G., Crăcan A., *Enhanced Wide Range Tunable CMOS Transconductor for Signal Processing*, Romanian J.of Information Sci. and Technol., **4**, 313-330 (2017).

Bonteanu G., Crăcan A., *Wide Range Electrically Controlled CMOS Transconductor for Adaptive Signal Processing*, Internat. Semiconductor Conf. (CAS), 2017, pp. 301-304.

Palmisano G., Pennisi S., *New CMOS Tunable Transconductor for Filtering Applications*, The IEEE Internat. Symp. on Circ. and Syst., 2001, pp. 196-199.

Pavan S., Tsividis Y., *High Frequency Continus Time filters In Digital CMOS Process*, Kluwer Academic Publishers, 2002.

Toumazou C., Ledge F.J., Haig D.G., *Analogue IC Design: the Current-Mode Approach*, Peter Peregnirus Ltd, London, UK, 1990.

UTILIZAREA OGLINZILOR CU CÂŞTIG CONTROLAT ELECTRIC ÎN REALIZAREA TRANSCONDUCTORILOR AJUSTABILI

(Rezumat)

Prezenta lucrare este o discuție extinsă relativ la utilizarea oglinzilor de curent cu câştig controlat electric în implementarea amplificatoarelor transconductanță ajustabile. Sunt studiate în paralel două soluții de realizare a oglinzilor cu factor de câştig controlat electric publicate anterior şi sunt trecuți în revistă prametri de interes precum domeniul de ajustare, gama dinamică, liniaritatea şi zgomotul. Ambele soluții de circuit se bazează pe comportamentul unor amplificatoare de curent ce utilizează două arhitecturi de oglinzi de curent dezechilibrate controlat.