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A REVIEW OF THE TRANSCONDUCTANCE CONTROL SOLUTIONS

BY

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Abstract. This paper briefly presents several transconductance control solutions in CMOS implemented G_m-C filters. Starting from the common control of the transconductance through the bias current and passing through gain control through degeneration, modern control solutions using electrically controlled gain current mirrors, negative feedback loops or pseudo-differential stages are reviewed.

Key words: transconductor; OTA; tunable transconductance.

1. Introduction

The use of transconductance amplifiers began in the 60's when one of the leaders of the linear semiconductor market has launched the CA3080 integrated circuit. These devices serve a very useful function that is being implemented on a regular basis in many integrated circuits as an element for more advanced purposes (Ramus, 2009).

Advantages such as the much wider frequency range or the possibility of manufacturing on the same semiconductor chip on which the numeric nucleus is integrated have forced the conversion from OPAMP-RC circuit solutions to some transconductor-capacitor solution the for analogue signal processing.

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The problem of transconductance control is as old as the use of transconductors in implementing G_m-C filters. Whether we are talking about the variation with the process of CMOS capacitors or about the inherent variation with the process and the temperature of the transconductance itself, there is a need to adjust the gain of the transconductance operational amplifier. The excellent versatility of this kind of control is given by the fact that, in addition to the need to compensate its own drifts with the process or temperature, the adjustability of the transconductance contributes to controlling the poles of filter that they implement.

2. Transconductance Control Solutions

We can mainly talk about two ways to get adjustable transconductors: open loop control methods and control methods that use a negative feedback loop.

In the open loop control class, we distinguish control solutions based on bias current transconductance dependence (Khorramabadi, 1984; Kaewdang, 2014), control solutions based on degeneration resistance adjustment (Czarnul, 1986; Mensink, 1997; Sanchez-Rodriguez, 2008), solutions using a pseudo-differential stage (Calvo, 2006) and solutions using electrical controlled gain current mirrors (Palmisano, 2001).

From the class of closed loop control methods, we will present solutions using a linear region biased input transistor (Sanchez-Rodriguez, 2014) and solutions using active devices on the input stage (Sănduleanu, 1998).

3. Achieving Adjustable Transconductance by Controlling the Bias Current

The natural way to control the gain of a CMOS implemented transconductor is of course through the bias current (Khorramabadi, 1984), as shown in Fig. 1.

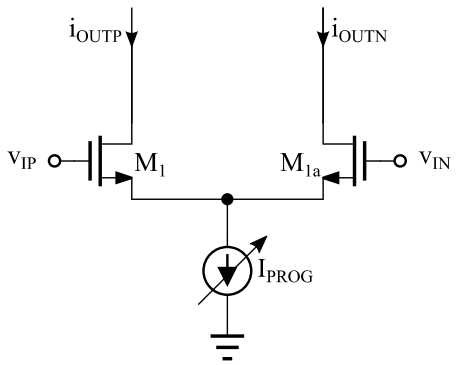

Fig. 1 – Tunable transconductor by bias current adjustment.

For the structure shown in Fig. 1 the transconductance will be given by:

$$g_m = \sqrt{2KI_{\text{PROG}}}.$$

Although achieving such control is very easy to implement, there are a number of disadvantages:

– given the dependence of the transconductance on the control current, for a desired control range, the control current must be varied in a more extended (quadratic) range;

– various interest parameters of the transconductor, such as the input dynamic range, dynamic range at the output and output resistance, will be affected by the change in bias current.

3. Achieving Adjustable Transconductance by Controlling the Bias Current and Squaring g_m

In Kaewdang, (2014) a solution is proposed to eliminate the disadvantage of the square extended control current range by using a transconductance squaring technique in order to obtain a linearly adjustable transconductor, as shown in Fig. 2.

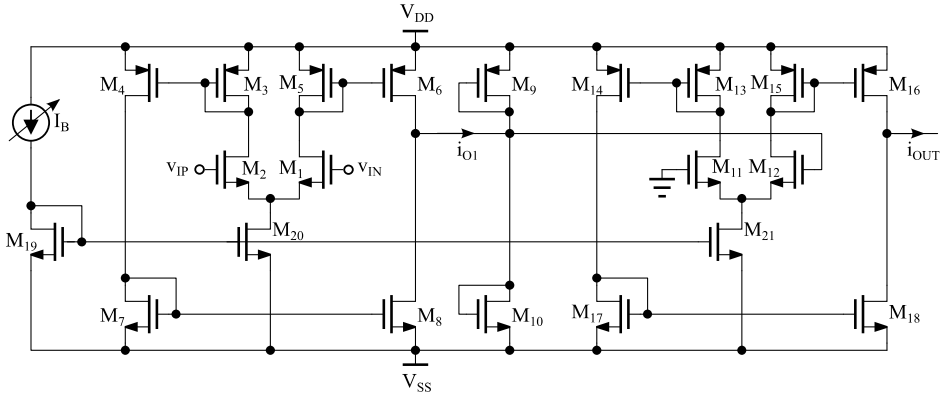

Fig. 2 – Implementation of bias current linear dependent transconductance.

For the left side of the Fig. 2 structure transconductance amplifier, one can write:

$$g_{m1} = \frac{\mathrm{d}i_{o1}}{\mathrm{d}v_i} = \sqrt{2KI_B}.$$

The voltage drop on M_9 – M_{10} transistor implemented active resistor will be:

$$v_R = i_{o1}R = g_{m1}v_iR.$$

The right side transconductor output current will be:

$$i_{\text{OUT}} = g_{m2} v_R = g_{m1} g_{m2} R v_i.$$

It remains that the transconductance of the entire structure is:

$$g_m = g_{m1} g_{m2} R = \alpha I_B.$$

The last relationship clearly indicates that the presented transconductor gain can be electrically and linearly adjusted by the bias current I_B. The implementation of the (Kaewdang, 2014) structure allowed the transconductance to be adjusted over a 3 decade range under the bias current variation in a 5 decade range.

4. Achieving Adjustable Transconductance by Controlling the Degeneration of a Differential Stage Using Transistors in the Linear Region

Controlling transconductance by adjusting the degree of degeneration of a differential input stage using MOS transistors biased in the linear region as degeneration resistors was first proposed in (Czarnul, 1986) in the form shown in Fig. 3.

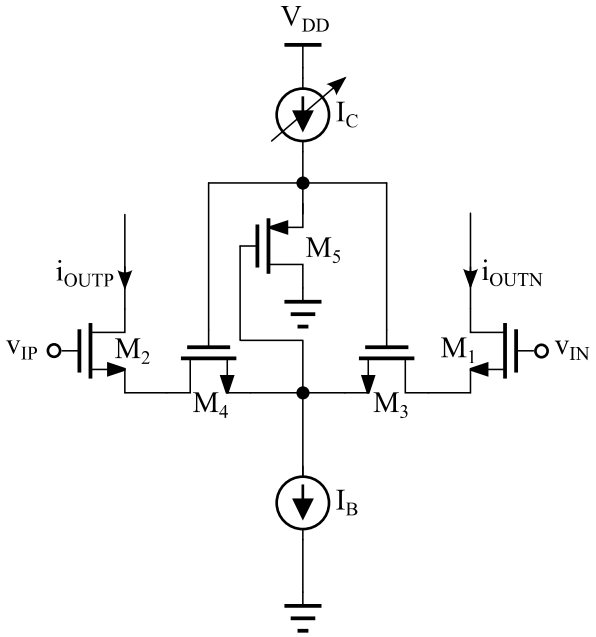

Fig. 3 – Implementation of adjustable transconductors by controlling the degeneration of a differential stage using transistors in the linear region.

The output current will be given by:

$$i_{OD} = \frac{1}{2}\left(i_{OUTP} - i_{OUTN}\right) = \frac{1}{2}\left\{G_C\left(v_{IP} - v_{IN}\right) - g\left(v_{IP} - v_{GS1}\right) + g\left(v_{IN} - v_{GS2}\right)\right\},$$

$$G_C = 2K_N\left(V_C - V_{THN}\right),$$

$$V_C = \sqrt{\frac{I_C}{K_P}} + V_{THP},$$

where: $K_N = K_2 = K_4$ and $g(V)$ is a nonlinear control independent function.

This solution provides a sufficient range of control to compensate for process variations and temperature variations, while also allowing large amplitude signal processing.

5. Achieving Adjustable Transconductance by Continuously Adjusting Degeneration Resistance Using Switches Implemented with Transistors in Controlled Resistor Mode

One possibility of achieving a continuously adjustable transconductor is to use a differential stage with adjustable degeneration resistances (Mensink, 1997). This solution is suitable for implementation in deep submicron CMOS technologies, being almost insensitive to 2nd order MOS effects such as the carriers' reduced mobility or velocity saturation. The degeneration resistors are soft switched by switches implemented with MOS transistors biased in controlled resistor mode as shown in Fig. 4 for an architecture where two such switches are used.

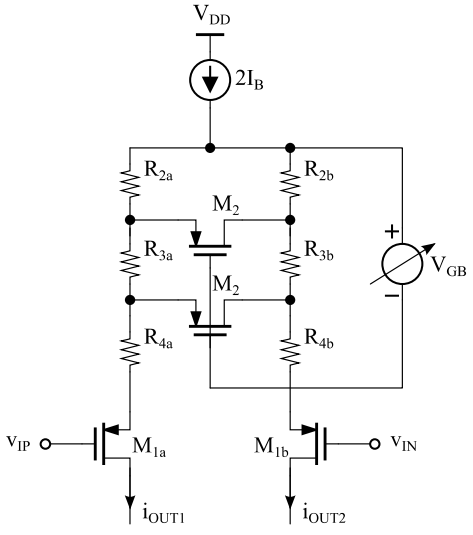

Fig. 4 – Adjustable transconductor by continuous adjustment of degeneration resistance using soft switches implemented with transistors in controlled resistor mode.

Adjustment of transconductance is achieved by V_{GB} voltage. The degeneration resistance can be gradually varied by means of the soft-switched transistors M_2 and M_3, thus obtaining a continuously adjustable transconductance. Although the gates of the M_2 and M_3 transistors are connected to the same potential, due to the R_2I_B voltage drop on the resistors $R_{3a,b}$, the gate-source voltages of the two transistors will meet: $V_{GS2} > V_{GS3}$. Consequently, M_2 will always be in conduction ahead of M_3 thanks to the substrate effect. For low V_{GB} control voltage values, the two M_2 and M_3 switches are cutoff so that degeneration resistance is maximal, $R_{\text{DEG\_MAX}} = R_2 + R_3 + R_4$. For a slightly higher control voltage, M_2 will begin to conduct and will shunt some of the $R_{2a,b}$ resistance. At higher values of the control voltage M_3 will start to conduct and will shunt some of the $R_{3a,b}$ resistance. The minimum degeneration resistance will be given by $R_{\text{DEG\_MIN}} = r_{ds3} + R_4$.

For a sufficiently high degeneration resistance value, the differential stage currents will be given by:

$$\begin{cases} i_{\text{OUT1}} = I_B + \dfrac{v_{ID}}{2R_{DEG}}, \\ i_{\text{OUT2}} = I_B - \dfrac{v_{ID}}{2R_{DEG}}. \end{cases}$$

If there is no further multiplication of the currents up to the output nodes, the equivalent transconductance of an OTA to use this input stage will be given by:

$$G_m = \frac{\partial i_{od}}{\partial v_{id}} = \frac{1}{R_{\text{DEG}}}.$$

Besides the obvious advantages of the presented structure given by the implementation simplicity, we must mention the drawback given by the necessity of a tradeoff between the maximum allowed amplitude at the transconductor input and the control range, since a sufficiently large differential voltage will cause saturation of the switches and so distortions will result.

6. Achieving Adjustable Transconductance by a High Linearity Degeneration Active Resistance Continuous Adjustment

Another possibility of achieving adjustability in transconductors, which is also based on the input stage degeneration principle, is to use as degeneration resistor a quasi-floating gate transistor (QFG), as shown in Fig. 5. Using QFG transistors, a linearity of the transconductor comparable to that resulted from a passive degeneration resistor usage is achievable (Sanchez-Rodriguez, 2008).

The degeneration structure uses linear region transistors whose equivalent resistance is adjusted by the V_{PROG} gate voltage. The essential difference compared to the case when using a simple triode transistor is given by the fact that the control voltage is applied by means of high resistors, R_{LARGE},

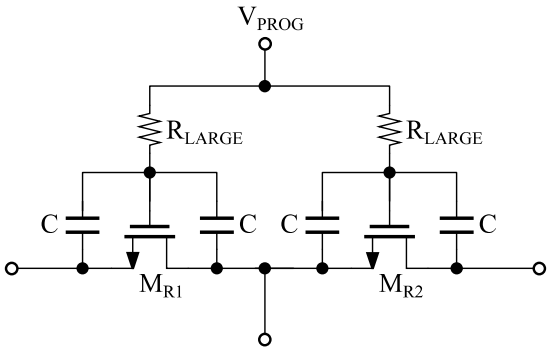

Fig. 5 – Active degeneration resistance implemented with QFG transistor.

so the potential of the gate can vary. This way, the drain and source AC voltage components are applied to the gate via the capacitive divider, which causes the cancelation of the v_{ds}^2 non-linear dependence of the triode region operating transistor drain current:

$$v_{gs} = \frac{v_{ds}}{2} \Rightarrow i_d(v_{ds}) = K\left[\frac{v_{ds}^2}{2} - \frac{v_{ds}^2}{2}\right] = 0.$$

The R_{LARGE} high resistance element can be implemented using either a transistor connected as a diode or a sub-threshold region biased transistor.

7. Achieving Adjustable Transconductors by Continuous Adjustment in a Pseudo-Differential Stage

Although attractive for implementation ease, the transconductance control solutions based on the modulation of the differential input stage degeneration as well as those controlling the bias current suffer from an important drawback: the control influences the dynamic range of the input voltage, additional circuits being required to adjust the common mode voltage at the input along with the electrical control of the transconductance. In Calvo, (2006) a possible solution is proposed, as shown in Fig. 6.

Each transistor in the pseudo-differential stage is made up of two matched transistors, $M_{1A} - M_{1B}$ and $M_{2A} - M_{2B}$. The input signals are applied to the M_{1A} and M_{2A} transistors acting as source followers enhanced by the negative feedback loops made with M_{31} and M_{32}. As a result, the input signals are transferred into the M_{1B} and M_{2B} transistors, which have the gates driven by the same voltage $V_{CM} + V_{\text{GAIN}}$. Due to the fact that the M_{1A} and M_{1B} transistors are matched and have identical geometries, the continuous current through M_{1B} will replicate the M_{1A} one, but with a gain that will depend on the voltage V_{GAIN}.

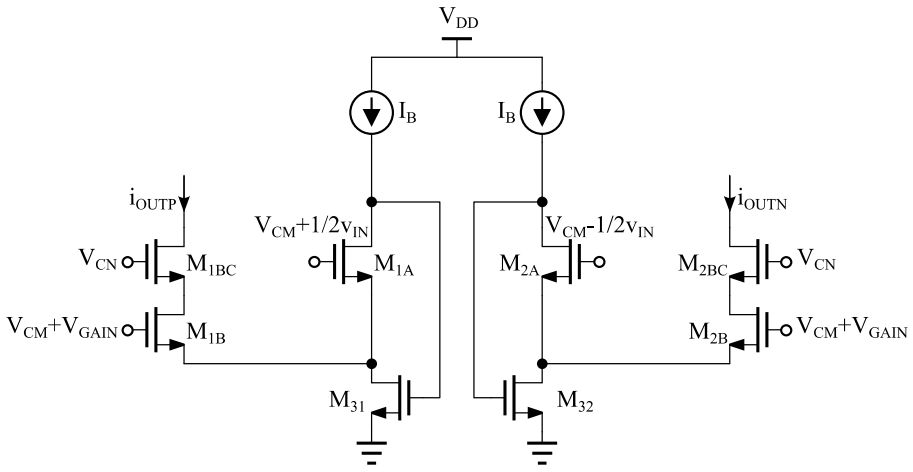

Fig. 6 – Transconductance control in a pseudo-differential stage.

Current changes of M_{1B} will be taken over by M_{31}. This results in a differential output current given by:

$$i_{OD} = i_{\mathrm{OUTP}} - i_{\mathrm{OUTN}} = 2K\left(V_{CM} + V_{\mathrm{GAIN}} - V_{TH}\right)v_{\mathrm{IN}},$$

where: V_{TH} is the threshold voltage for M_B and

$$K = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_B .$$

The structure shown is therefore able to maintain the V_{CM} common mode input voltage constant when the transconductance is controlled by V_{GAIN}. The presented method allows only a 1:2 transconductance adjustment range in good linearity conditions.

8. Adjusting Transconductance by Using Electrically Controlled Gain Current Mirrors

A solution to obtain electrically controlled transconductance based on the use of electronically controlled gain current mirrors (Palmisano, 2001) is shown in Fig. 7.

The M_1 transistor acts as a source follower with improved accuracy, being biased with a constant I_{B1} current, thanks to the $M_2 - M_3 - M_4$ enclosed negative feedback loop. Considering the same geometrical factor for $M_2 - M_3 - - M_4$, the input transistor equivalent transconductance can be written as:

$$g_{m1eq} = g_{m1}\left(\frac{1}{2}g_{m2}r_{01}\right).$$

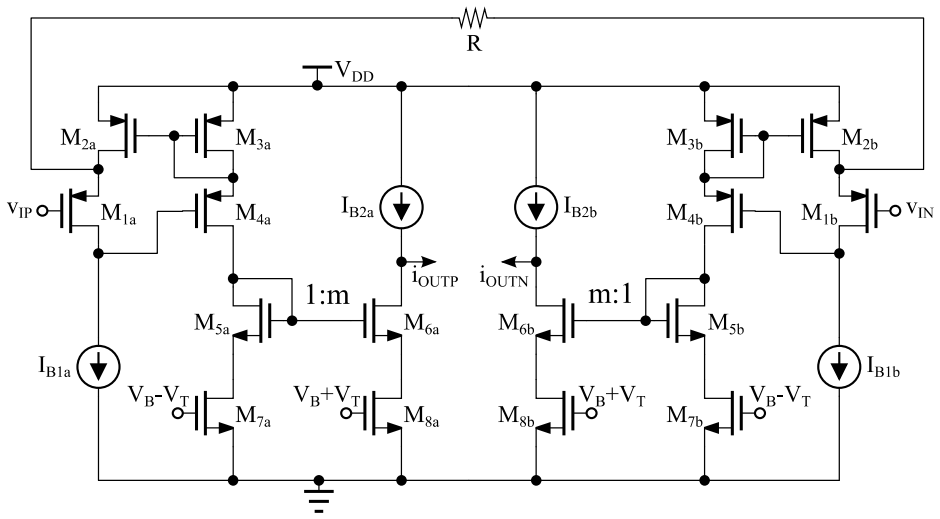

Fig. 7 – Control of transconductance by use of electrically controlled gain current mirrors.

Applying a differential voltage v_{ID} between inputs, a v_{ID}/R current will flow through the resistor R. This current can only be injected by M_2, it is then copied by M_2 and thus provided to the $M_5 - M_6$ gain mirror input. At the transconductor output this current will be multiplied by the á mirror adjustment factor. Since the mirror-adjusting factor also multiplies the DC value, the implementation requires a multiplication with the same factor of the bias current so that the unwanted DC level in the output to be rejected.

The $M_7 - M_8$ transistors are biased in the linear region and act as voltage-controlled degeneration resistors for the $M_5 - M_6$ current mirror. For $v_{DS} << (V_{GS} - V_{TH})/2$, the expression of the drain current in the triode region is given by:

$$i_D = 2K(V_{GS} - V_{TH})v_{DS}.$$

The equivalent conductance of the two triodes used for the current mirror degeneration will be:

$$G_{ds7} = 2K(V_B - V_T - V_{TH}); \quad G_{ds8} = 2K(V_B + V_T - V_{TH}).$$

For positive values of V_T the current factor $\alpha > m$ and for negative values $\alpha < m$. However, there is a need for a tradeoff between the adjustment range and the linearity of the transconductor. Also the dependence of the transconductance on the control voltage is not linear.

9. Performing Transconductance Control by the Action of a Negative Feedback Loop with Input Transistors in the Linear Region

In Sanchez-Rodriguez, (2014) an adjustable transconductor solution is shown where the input transistor is biased in the linear region, as shown in Fig. 8.

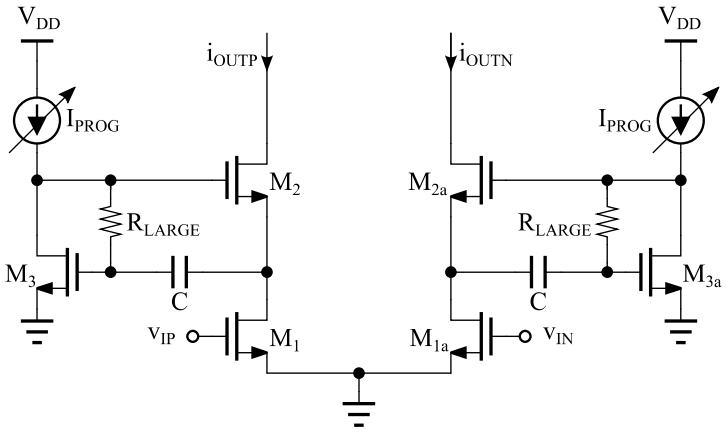

Fig. 8 – Preudo-differential stage where the input transistor is biased in the linear region.

The transconductor topology presented is a telescopic one, the linearity being improved by the regulated cascode technique: the drain-source voltage of the transistors operating in the triode region is kept as constant as possible. The extra gain stage, implemented with M_2, R_{LARGE} and C, has a multiple role:

– enclose a negative feedback loop that increases the actual gain of the cascode transistor, thus improving the output resistance as well as the gain of the transconductor;

– allows the use of input transistor drain-source voltages lower than a threshold voltage;

– by quasi-floating gate technique (QFG), DC input/output levels are decoupled, thus increasing the adjustment range;

The programmability of the transconductance is ensured by the bias current of the amplifier that performs the local feedback. However, the present structure calls for the existence of a complex circuit for common mode control since the common mode component of the input voltage modulates the common mode value of the current and the transconductance respectively. The expression of the drain current of the input transistor in the situation of its bias in strong inversion and linear region will be:

$$i_D = K_1\left[\left(v_{GS1} - V_{TH}\right)v_{DS} - \frac{v_{DS}^2}{2}\right].$$

But v_{GS1} is actually the input voltage, $v_I = V_{ICM} + v_i$, so the large signal transconductance will be:

$$G_m = \frac{i_{\text{OUT}}}{v_{ID}} = K_1 V_{DS1} = K_1 \left(V_{GS3} - V_{GS2}\right) = K_1 \left(\sqrt{\frac{I_{\text{PROG}}}{K_2}} - \sqrt{\frac{I_{CM}}{K_3}} \right).$$

10. Performing Transconductance Control by the Action of a Negative Feedback Loop with Saturation Region Biased Input Transistors

The key issue in analog signal processing under a low power supply voltage is the reduction of the dynamic range. Therefore, the extended range of adjustment required in CMOS transconductors to compensate for process and temperature variations typically conflicts with dynamic range requirements. A structure (Sanduleanu, 1998) which aims to solve this complicated equation is shown in Fig. 9.

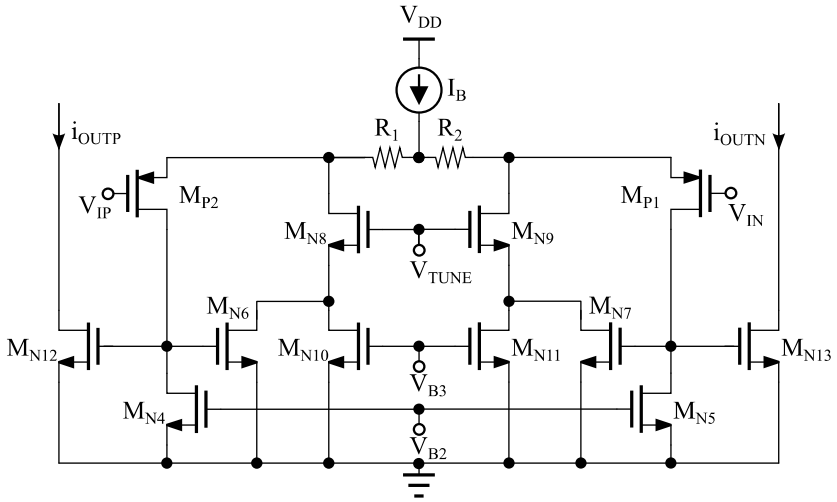

Fig. 9 – Transconductance control solution while keeping the input dynamic range.

The core of the transconductor consists of the differential stage implemented with $M_{P1} - M_{P2}$ PMOS transistors which benefit from a resistive degeneration implemented with $R_1 - R_2$ resistors. The differential input stage is biased with a constant current through the $M_{N4} - M_{N5}$ transistors by the $M_{N6} - M_{N10} - M_{N8}$ enclosed negative feedback loop. If the gain on this loop is high, the differential input voltage will be transferred to the degeneration resistors given that input PMOS transistors will act as source followers. Any variation of input voltage will be detected by the M_{N6} gate whose drain current will be divided between M_{N8} and M_{N10}, so that only a fraction of the current through M_{N6} will flow through the degeneration resistors. Since M_{N10} works in the linear region, its equivalent output resistance value will give the division ratio. Output

transistors $M_{N12} - M_{N13}$ will copy the $M_{N6} - M_{N7}$ current. The equivalent transconductance of the presented structure will be given by:

$$g_{mech} \cong \frac{g_{m12}}{g_{m6}} \cdot \frac{1}{R_1} \cdot \frac{1+g_{m8}r_{ds10}}{g_{m8}r_{ds10}}.$$

It can be seen that the transconductance can be adjusted continuously, varying the resistance of the $M_{N10} - M_{N11}$ triodes, but also in discrete steps, varying the $M_{N12} - M_{N13}$ aspect factor. When the V_{TUNE} control voltage changes, the loop reacts by maintaining the $M_{N8} - M_{N9}$ gate-source voltages constant, so that the $M_{N10} - M_{N11}$ equivalent resistance and the equivalent transconductance of the structure to be directly controlled from the control voltage. The main advantage of the presented structure is the independence of voltage drop on the degenerate resistors to the V_{TUNE} voltage, but the continuous tune range is nevertheless reduced.

11. Conclusions

This paper is intended to be a review of the main methods of transconductance control for the G_m-C filters implemented in CMOS technologies. Both open loop control methods and closed loop control methods are reviewed. Starting from bias current control, there are presented control methods based on the degeneration of a differential input stage, methods using electrically controlled gain current mirrors, and methods that turn to pseudo-differential stages. Control of transconductance can come directly or by the action of a negative feedback loop. Methods of improving the linearity and the input dynamic range respectively are also presented.

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O TRECERE ÎN REVISTĂ A METODELOR DE CONTROL ALE TRANSCONDUCTANȚEI

(Rezumat)

Această lucrare se doreşte a fi o trecere în revistă a principalelor metode de control ale transconductanței în cazul filtrelor G_m-C implementate în tehnologiile CMOS. Sunt trecute în revistă atât metode de control în buclă deschisă cât şi metode de control în buclă închisă. Pornind de la controlul prin curentul de polarizare, se prezintă apoi metode de control bazate pe degenerarea unui etaj diferențial, metode ce folosesc oglinzi cu câştig controlat electric dar şi metode ce apelează la etaje pseudo-diferențiale. Controlul transconductanței poate parveni direct sau prin acțiunea unei bucle de reacție negativă. Sunt prezentate deasemenea metode de îmbunătățire a liniarității şi respectiv a gamei dinamice la intrare.