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COMPARISON BETWEEN DC-AC TOPOLOGIES WITH THREE VOLTAGE LEVELS

BY

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Abstract. In this paper a comparison between DC-AC topologies with three voltage levels (3L) is presented. This comparison takes into account the most popular 3L topologies (NPC: Neutral-Point-Clamped, FC: Flying-Capacitor, CI: Coupled-Inductor) and 3L-MMC (Modular-Multilevel-Converter) technology. In order to evaluate the performances of these topologies, the half-bridge circuit with the same number of active power devices is used. The parameters considered in this comparison are: voltage/current switched by power devices, the apparent switching frequency of the output voltage and the existence or not of passive components that require a high switching frequency.

Key words: multilevel inverters; NPC structure; Flying-Capacitor concept; Coupled-Inductor principle and MMC topology.

1. Introduction

The interest of voltage-source-inverters (VSI) in multilevel technology has continuously increased. This is mainly due to their advantages for medium-voltage (MV) applications, such as: reducing the switched voltage/current and improving the quality of the output waveforms. The multilevel VSI topologies are used in a wide range of applications, such as flexible AC transmission systems (FACTS), reactive power compensation, pumps, rolling mills, conveyors, renewable energy systems, industrial motor drives etc. There are many multilevel topologies and most of them are based on a primary DC source

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and two secondary sources composed of two capacitor banks (Kouro *et al.*, 2010).

Recently a new multilevel energy conversion technology has been developed for direct connection to the high-voltage (HV) grid. This principle is different from VSI multilevel technology and was named Modular-Multilevel-Converter (MMC) (Lesnicar, 2003). The MMC technology (Fig. 1) is also applicable for medium-voltage (MV) applications. Among the advantages of this concept are mentioned: quasi-sinusoidal AC voltage waveform, lower harmonic content, reduced costs for filtering, higher modularity and higher efficiency.

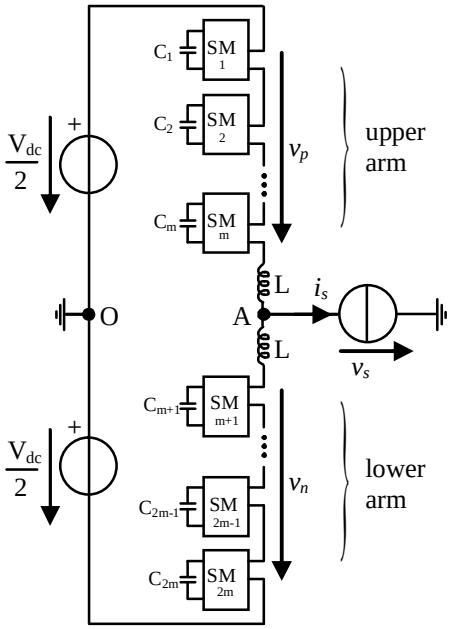

Fig. 1 − Single-phase half-bridge NL-MMC topology.

Until recently, the multilevel VSI technology has dominated the market of energy conversion. At the same time with the adoption of MMC technology by industry, the MMC principle has become a major competitor for multilevel VSI topologies. MMC concept uses a low switching frequency, which enables to switch high currents with low switching losses. Therefore, MMC technology is gaining momentum in various applications such as high-voltage direct-current (HVDC) transmission schemes and flexible AC transmission systems (FACTS) (Sharifabadi, 2016).

Over time, various simulation models for the MMC concept have been developed. In the paper (Solas, 2010) the power devices are considered as ideal switches, while in the work (Abildgaard *et al.*, 2012, 2016) the valves was

treated as two-state resistive devices with low resistance when switched on and high resistance in the off state.

In this paper a comparison between DC-AC topologies with three voltage levels is presented. This study takes into account the most popular 3L topologies (Neutral-Point-Clamped, Flying-Capacitor, Coupled-Inductor) and cascade connecting of switching cells (Modular-Multilevel-Converter).

The work is organized as follows. In Section **2** the basic of three 3L topologies (Neutral-Point-Clamped, Flying-Capacitor and Coupled-Inductor) with the same number of active power devices is presented. Section **3** briefly shows the MMC principle. Compared to other topologies of multilevel converters, the multilevel MMC topology has a complex internal dynamics. Thus, the specific equations are also explained. In Section **4** modelling of 3L-MMC topology is shown. Finally, the conclusions are summarized.

2. Three Voltage Levels DC-AC Topologies

3L-NPC topology

Fig. 2 presents the half-bridge three-level Neutral-Point-Clamped (3L-NPC) inverter. The main DC voltage source U_{dc} is divided into two secondary sources, made by capacitors C_1 and C_2. The midpoint of the capacitors (O) is used to achieve the intermediate voltage level.

The 3L-NPC structure contains four bipolar power switches (S_1, S_{1c}, S_2 and S_{2c}) and a tripolar power switch (D_c). The bipolar switches are bidirectional in current, while the three-pole power device contains two unidirectional states. All semiconductor devices support half of the continuous supply voltage ($U_{dc}/2$).

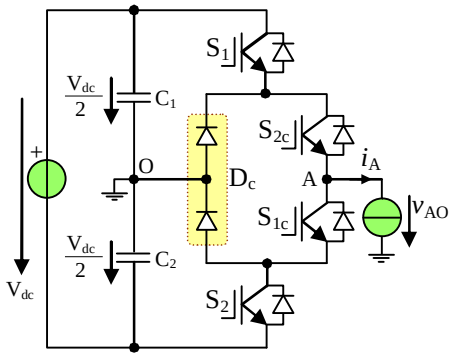

Fig. 2 − Single-phase half-bridge 3L-NPC inverter.

Using the Level-Shifted (LS)-SPWM strategy it is observed that the 3L-NPC structure has three voltage levels ($U_{dc}/2$, 0 and $-U_{dc}/2$) and three switching sequences. The power switches S_1 and S_{1c}, respectively S_2 and S_{2c}, are complementarily controlled throughout the cycle. One cycle is represented by

the reference voltage period. As a result of the intermediate voltage level, the ripples current are reduced by half compared to the classical two voltage levels (2L) structure. Another advantage is the switched voltage of power devices, which is also reduced by half.

The control of power switches depends on the reference voltage signal. If the reference voltage is positive, the power devices S_1 and S_{1c} switch to the switching frequency (f_{sw}), while S_2 is turned off and S_{2c} is turned on. When the reference voltage is negative, the power devices control is reversed: S_2 and S_{2c} are complementary controlled at f_{sw}, while S_1 is turned off and S_{1c} is turned on. As a result, the apparent (effective) switching frequency (f_{ap}) of the output voltage is equal to f_{sw} ($f_{ap} = f_{sw}$).

The clamp diodes form the tripolar power switch (D_c) and work complementary with outer power devices (S_1 and S_2). Replacing the unidirectional power switch (D_c) with two other types of tripolar switches, two other three-level structures (3L-Vienna and 3L-Active-NPC) have been obtained.

3L-FC topology

In Fig.3 the single-phase half-bridge 3L-FC inverter is presented. The main DC voltage source U_{dc} is also divided into two secondary sources, made by capacitors C_1 and C_2. The median point (O) of the capacitor battery is connected to the load.

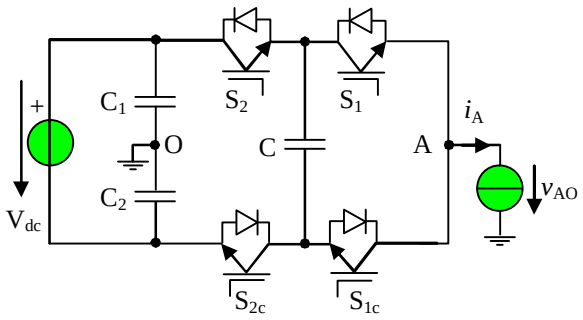

Fig. 3 − Single-phase half-bridge 3L-FC topology.

The 3L-FC topology contains four bipolar power switches (S_1, S_{1c}, S_2 and S_{2c}) which form two switching cells *series* connected. An intermediate capacitor (C) is connected between the cells. It is charged at half of continuous supply voltage ($U_{dc}/2$). Phase-shifted (PS)-SPWM principle is used to control the switching cells. Thus, four switching states denoted P, O_1, O_2 and N, are obtained. The O_1 and O_2 states are redundant states for which the output voltage is zero. These states allow doubling the apparent switching frequency at the output of the converter ($f_{ap} = 2f_{sw}$). The other states, P and N, allow the load to be connected to the positive or negative terminal of the supply voltage. Thus,

the output voltage has three voltage levels ($U_{dc}/2$, 0 and $-U_{dc}/2$) and the voltage across semiconductor devices is half the continuous supply voltage ($U_{dc}/2$).

3L-CI topology

The 3L-CI structure (Fig.4) contains four bipolar power switches (S_1, S_{1c}, S_2 and S_{2c}) which form two switching cells *parallel* connected. Between the cells a coupled-inductor (CI) is connected. PS-SPWM principle can also be used to control the switching cells.

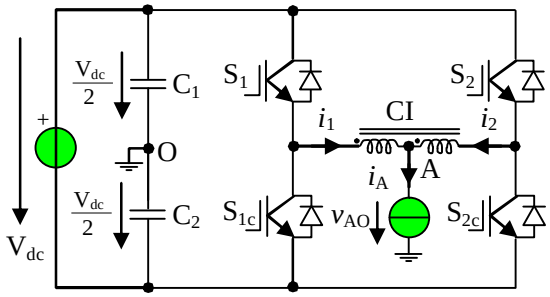

Fig. 4 − Single-phase half-bridge 3L-CI topology.

The currents through CI windings (i_1 and i_2) are half of the load current ($i_A/2$). Thus, the currents flowing through the power switches (S_1, S_{1c}, S_2 and S_{2c}) are equal to half the load current. The switched voltage of the power devices is equal to the continuous supply voltage (U_{dc}), similar with 2L-VSI topology.

The output voltage has three voltage levels ($U_{dc}/2$, 0 and $-U_{dc}/2$) and the apparent switching frequency of the output voltage is twice the switching frequency ($f_{ap} = 2f_{sw}$).

3. Basic MMC Topology

The MMC technology performs a static conversion between a voltage source and a current source. The phase leg consists of two arms (upper and lower), which consist of *m* cascade-connected submodules (also called *cells*) and an inductor L. The submodules can be considered as variable voltage sources. Thus, the sum of these voltages gives the inserted voltages v_p and v_n. To avoid the direct connection of two voltage sources, one inductor L is inserted on each arm. In order to develop a mathematical model, this inductance contains a resistive part (R) and an inductive part (L). For *m* equal to 1 the topology with three voltage levels is obtained (Fig. 5). R_d represents the resistance in conduction of power devices and connecting wires for one arm.

The SM_1 and SM_2 cells consist of a half-bridge circuit with two power devices: S_1-S_{1c} and S_2-S_{2c}. Each one of the switches consists of a controllable

semiconductor device – generally a power transistor, *e.g.* an insulated-gate bipolar transistor (IGBT) with an anti-parallel-connected diode. The control of active power devices is complementary. They can be turned off at the same time (during the dead time), but can not be in conduction at the same time. When a power device is turned on, either the transistor or the anti-parallel diode will conduct, depending on the current direction. Each submodule is equipped with a capacitor (C_p, C_n), which is connected across both switches. These capacitors are charged at the continuous supply voltage U_{dc}. Thus, the switched voltage of power devices is equal with U_{dc}, similar with 2L-VSI topology.

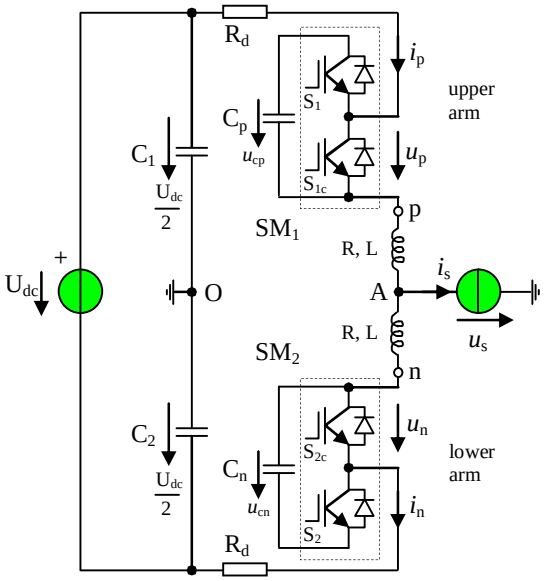

Fig. 5 − Single-phase half-bridge 3L-MMC topology.

4. Dynamic Relations and Control of 3L-MMC Topology

By using *m* submodule on each arm a power structure with *N* voltage levels can be obtained ($N = 2m + 1$) (Fig.1). In order to present the specific equations of MMC principle, it was considered one submodule per arm (Fig. 5).

In accordance with the circuit, the currents fulfill the equation (1). The average current along the phase i_{pn} is defined as half of the two arm currents (i_p, i_n) sum, as expressed in (2).

$$i_s = i_p - i_n, \tag{1}$$

$$i_{pn} = \frac{i_p + i_n}{2}. \tag{2}$$

Using equations (2) and (3) the currents on each arm are calculated:

$$i_p = i_{pn} + \frac{i_s}{2}, \tag{3}$$

$$i_n = i_{pn} - \frac{i_s}{2}. \tag{4}$$

The dynamic relations of the MMC topology are expressed for the upper and lower arms in (5).

$$\begin{cases} u_s - \frac{U_{dc}}{2} + R_p i_p + u_p + R i_p + L\frac{\mathrm{d}i_p}{\mathrm{d}t} = 0, \\ u_s + \frac{U_{dc}}{2} - R_n i_n - u_n - R i_n - L\frac{\mathrm{d}i_n}{\mathrm{d}t} = 0, \end{cases} \tag{5}$$

where,

$$\begin{cases} u_p = u_{cp} \cdot f_1 \\ u_n = u_{cn} \cdot f_2 \end{cases} \tag{6}$$

It may be considered that:

$$\frac{u_{pn}}{2} = R \cdot i_p + L\frac{\mathrm{d}i_p}{\mathrm{d}t} = R \cdot i_n + L\frac{\mathrm{d}i_n}{\mathrm{d}t}. \tag{7}$$

In relations (6), the switching functions (f_1 and f_2) are replaced with their average values over a switching period. Thus,

$$\begin{cases} u_{p\_avg} = u_{cp} \cdot \alpha_p \\ u_{n\_avg} = u_{cn} \cdot \alpha_n \end{cases} \tag{8}$$

Replace the expression (8) in dynamic relations (5) and highlight the reference values.

$$\begin{cases} u_s^* - \frac{U_{dc}}{2} + R_d \cdot \tilde{i}_p + \alpha_p^* \cdot \tilde{u}_{cp} + \frac{u_{pn}^*}{2} = 0 \\ u_s^* + \frac{U_{dc}}{2} - R_d \cdot \tilde{i}_n - \alpha_n^* \cdot \tilde{u}_{cn} - \frac{u_{pn}^*}{2} = 0 \end{cases} \tag{9}$$

where: $\tilde{i}_p$, $\tilde{i}_n$, $\tilde{u}_{cp}$ and $\tilde{u}_{cn}$ are the measured values.

As a result, the following control is obtained:

$$\alpha_p^* = \frac{1}{\tilde{u}_{cp}}\left(\frac{U_{dc}}{2} - u_s^* - R_d \cdot \tilde{i}_p - \frac{u_{pn}^*}{2}\right)$$
$$\alpha_n^* = \frac{1}{\tilde{u}_{cn}}\left(\frac{U_{dc}}{2} + u_s^* - R_d \cdot \tilde{i}_n - \frac{u_{pn}^*}{2}\right) \quad (10)$$

Ideally, the u_{cp} and u_{cn} voltages are equal to U_d.

Thus, the reference voltage $\tilde{u}_{pn}^*$ can be calculated according to the diagram of Fig. 6 and $\tilde{i}_{pn}$ is calculated using the measured currents $\tilde{i}_p$ and $\tilde{i}_n$.

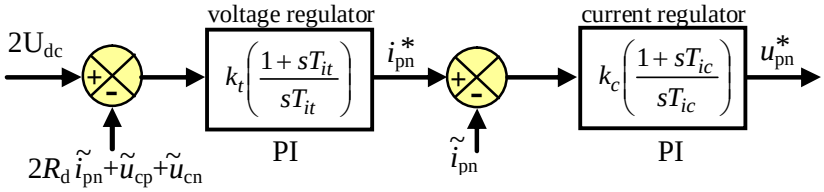

Fig. 6 − Block diagram of reference variables.

$$\tilde{i}_{pn} = \frac{\tilde{i}_p + \tilde{i}_n}{2} \quad (11)$$

In order to obtain the PWM strategy, the control variables (α_p^* and α_n^*) (Fig. 7) are compared with a carrier wave *c*.

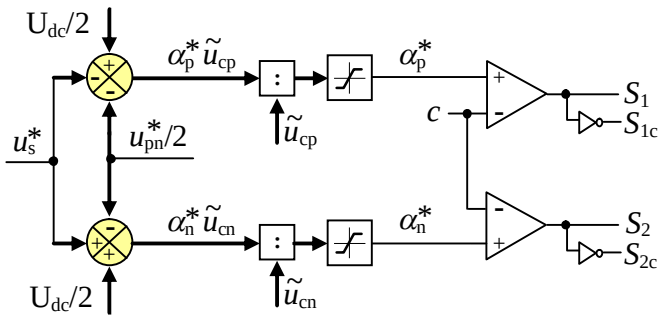

Fig. 7 − Block diagram of PWM strategy.

This PWM control has been implemented for 3L-MMC topology and some simulation results (output voltage – u_s, output current – i_s and u_{cp} and u_{cn} voltages) are shown in Fig. 8.

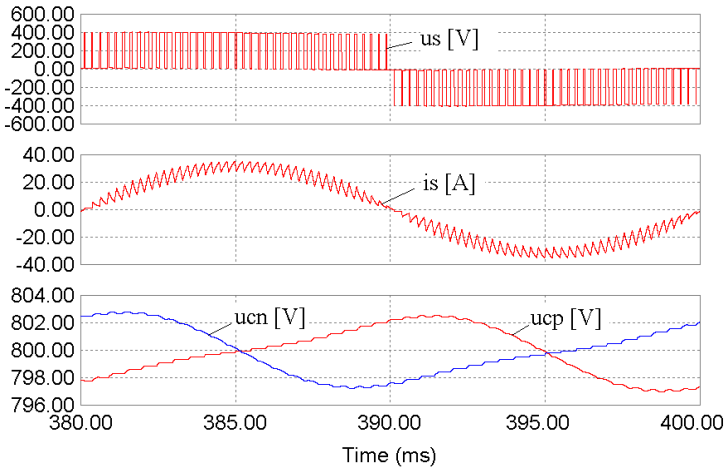

Fig. 8 − Simulation results for 3L-MMC topology
(U_{dc} = 800 V, M = 0.8 and f_{sw} = 2,000 Hz).

It is observed that the output voltage has three voltage levels ($U_{dc}/2$, 0 and $-U_{dc}/2$) and the apparent switching frequency is twice the switching frequency ($f_{ap}=2f_{sw}$).

5. Conclusions

In this paper a comparison between DC-AC topologies with three voltage levels has been presented. This comparison took into account the most popular 3L topologies (NPC, FC and CI) and 3L-MMC technology. In order to evaluate the performances of these topologies the half-bridge circuit with the same number of active power devices has been used. The parameters used in this study were: voltage /current switched by power devices, the apparent switching frequency of the output voltage and the existence or not of passive components that require a high switching frequency.

The 3L-NPC topology has the advantage that is simple and the power devices support a voltage equal to half of continuous supply voltage. The disadvantage of this structure is the unbalanced distribution of total power device losses. This inconvenience leads to limit of maximum output power and/or maximum switching frequency. The 3L-FC and 3L-CI concepts have the advantage of doubling the apparent switching frequency of the output voltage, but the presence of floating capacitors and coupled inductors require a high switching frequency which limits the applicative area of these topologies.

The MMC technology is different from voltage source inverters. This concept allows the cascade-connected of a very large number of submodules.

Thus, at the same time with the reduction of the switched voltage, the apparent switching frequency also increases. As a result, the switching frequency can be reduced and thus the switching losses are reduced compared to multilevel VSI concepts.

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COMPARAȚIE ÎNTRE CONVERTOARELE DC-AC CU TREI NIVELURI DE TENSIUNE

(Rezumat)

În această lucrare este prezentată o comparație între topologiile DC-AC cu trei niveluri de tensiune (3L). Această comparație ia în considerare cele mai populare structuri 3L (NPC: Neutral-Point-Clamped, FC: Flying-Capacitor, CI: Coupled-Inductor) şi tehnologia 3L-MMC (Modular-Multilevel-Converter). Pentru a evalua performanțele acestor convertoare se utilizează circuitul în semipunte cu același număr de dispozitive semiconductoare active. Parametrii considerați în acest studiu sunt: tensiunea/curentul comutat de dispozitivele semiconductoare de putere, frecvența aparentă de comutație a tensiunii de ieşire şi existența sau absența componentelor pasive care necesită o frecvență mare de comutație.