BULETINUL INSTITUTULUI POLITEHNIC DIN IAŞI
Publicat de
Universitatea Tehnică „Gheorghe Asachi” din Iaşi
Volumul 64 (68), Numărul 2, 2018
Secția
ELECTROTEHNICĂ. ENERGETICĂ. ELECTRONICĂ

ON PERFORMANCE ESTIMATION FOR A DC-DC BUCK CONVERTER BY MEANS OF DESIGN OF EXPERIMENTS

BY

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Received: May 21, 2018
Accepted for publication: June 29, 2018

Abstract. Design of Experiments (DoE) is a concept used in the context of “black-box” or “grey-box” approaches where the outputs of interest of a system are difficult to be expressed in a deterministic manner. This paper presents how the DoE can be used for estimating time-domain performances (overshoot and settling time) for a DC-DC Buck Converter. Contrary to the common polynomial approach, in this paper an estimator function based on a FFT (Fast-Fourier Transform) is used. This offers a better trade-off between the number of experiments required and accuracy. To validate the values obtained via FFT estimation, time-domain simulations of the nonlinear model of the application are provided. The proposed method can be applied either on the experimental setup or on simulation model (as in this work).

Key words: DC-DC Buck converter; performance estimation; fast fourier transform; design of experiments; PID control.

1. Introduction

Nowadays DC-DC converters are highly spread in many branches including industrial, automotive, medical and others, hence the need for developing high-performance applications in short-time frames. There are

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several key problems that should be discussed when developing such converters: dimensioning the output filter components (Erikson & Maksimovic, 2004), choosing the control method that meets the specifications of the application in which it will be integrated (Shahroki & Zomorrodi, 2012; Astrom & Hagglund, 2004; Abe *et al.*, 2011; Jia *et. al.*, 2010), tuning the control to assure on one hand stability (Garpinger & Hagglund, 2008) and on the other hand desired performances (Zhang *et. al.*, 2002; Kurokawa *et. al.*, 2010) as well as mechanisms to limit the nonlinear effects such as limit cycles (Peterchev *et al.*, 2003; Bradley *et al.*, 2011).

The paper focuses on the analysis of a DC-DC Buck converter controlled through a PID embedded algorithm. The target of the work is to obtain a good estimation of time-domain performances of the DC-DC Buck converter (such as overshoot and settling time) for different values of PID parameters in case of input and load step scenarios. These estimations are obtained via a DoE method which involves using a FFT transform.

In the following, we first describe the DoE basics, then we offer an overview of the application under study and afterwards we describe the step-by-step approach we used for obtaining good accuracy estimations for both overshoot and settling time. To validate the obtained results time-domain simulations are provided.

2. Basics of Design of Experiments

The DoE concept considers the system under study a black box as shown in Fig. 1.

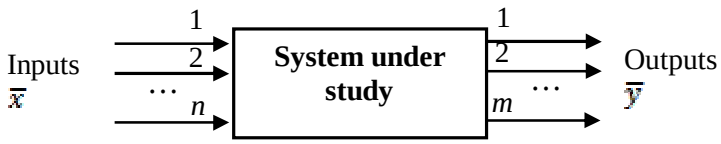


Fig. 1 – DoE Concept.

Let us assume that the inputs (also known as factors) are represented by the *n*-dimensional vector *x*, the outputs (responses) by the *m*-dimensional vector y and the function that correlates the inputs with the outputs is unknown. The aim of the DoE methods is to derive this unknown relation and express it in analytical form as:

$$\bar{y}_i = f_i\left(\bar{x}\right), \tag{1}$$

where: $i = 1,2,...,m$ and $\bar{x} = \left(x_1, x_2, \ldots, x_n\right)$.

The generic flow usually applied for building the DoE consists of the following steps (Montgomery, 2008): define the objectives of the experiment, choose the factors and the levels of variation, identify the responses of interest, choose the experimental design, execute the experiment, analyse the obtained

data and extract the empirical model in an often polynomial form. Throughout the years many experimental designs, such as: factorial, central composite, D-optimal, G-optimal, have been developed (Simpson *et al.*, 2001). These design types will define how the inputs of the system are varied throughout the experiment. To obtain a good estimation for the outputs of interest one should properly choose the mathematical model used for fitting the experimental data. In this direction there are available several fitting methods that can be applied, such as: least squares regression, weighted least squares regression, back-propagation etc. Once the expression of the function $f_i\left(\overline{x}\right)$ is known, a validation step is required to estimate the accuracy of the obtained model.

This kind of approach can be applied for a DC-DC Buck converter, using either simulation or measurement results. In this paper, we approximate the time-domain performances of the system for various parameter configurations of the PID control. For a DC-DC converter, it is of interest to evaluate the time-domain performances when either input step or load step scenarios are applied. Thus, it would be useful to approximate these performances through mathematical expression as in (1). The obtained functions can be furthermore used to calculate the dynamics of the converter for untested settings of the control; hence a fine tuning of the control can be achieved.

3. Application Overview

The block diagram of the DC-DC Buck converter under study is shown in Fig. 2.

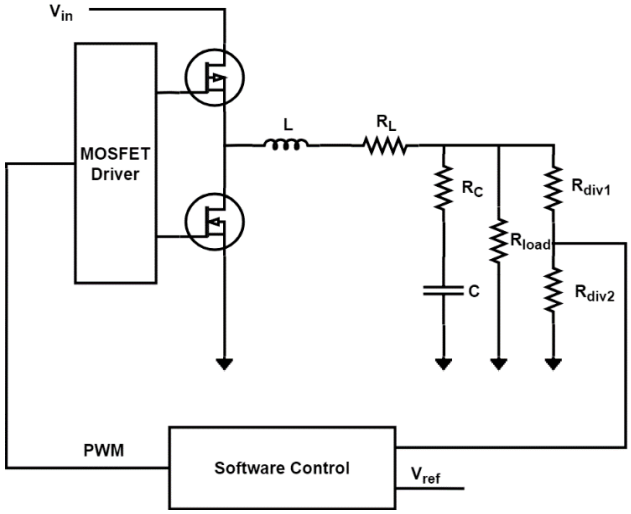


Fig. 2 – DC-DC Buck Converter – Block Diagram.

The above Buck converter consists of a half-bridge configuration (PMOS and NMOS) connected through an LC output filter to the load. The

MOSFET transistors are driven by two non-overlapping PWM signals operated at a frequency of 100 kHz. The load for the converter is assumed to be pure resistive. The control is done via a software PID algorithm embedded in a microcontroller. The reference voltage is fixed to a value of 5 V. The error between the output voltage and the reference voltage is supplied to the PID algorithm that in turn calculates the required duty cycle of the PWM signal to minimize the error. Since the control is discrete, a 12-bit ADC is used to convert the analogue output voltage to digital values.

For this converter two test scenarios are of interest: input step and load step. When these stimuli are applied at the input of the system, the output voltage will deviate from its steady state value (equal to 5 V in this case). The generic waveform exhibited by the output voltage is shown in Fig. 3, where the most important time-domain performances (overshoot and settling time) are highlighted.

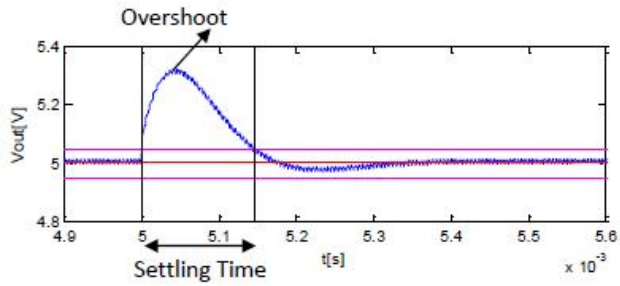


Fig. 3 – Time-domain performances.

The overshoot of any DC-DC converter can be calculated as the difference between the maximum value of the output response and the steady state value reached after the transient regime. The overshoot is usually expressed as percentages with respect to the steady state value. The settling time represents the time interval from the moment when the input/load step is applied and the moment when the output voltage reaches and remains within a vicinity of the steady state (Fig. 3).

For second order transfer functions, these performances can be easily expressed mathematically as in (Ghose, 2012). However, the behaviour of the DC-DC Buck converter in closed loop is defined by a 5^{th} order transfer function (Amariutei *et al.*, 2015a), hence it is impossible to determine mathematical expressions for overshoot and for settling time by means of algebraic manipulations not to mention the nonlinear case when this is in general impossible. The target of this work is to extract deterministic expressions of the performance by means of DoE.

All the experiments are done in simulations and the performances are automatically extracted from the output voltage waveform resulted after each simulation. The model used for the DC-DC Buck converter is a non-linear model built using the Simscape Toolbox from Matlab/Simulink. Nonlinear

effects such as quantization of the ADC and saturation of the PWM block are added to the model. The experiments are based on varying the values of the parameters: K_p , K_i , K_d (inputs for the black-box in Fig. 1) and calculating the values of the overshoot and settling time (outputs for the black-box in Fig. 1). The extracted function will depend only on the values of K_p , K_i , K_d since the rest of the parameters are imposed by hardware implementation.

4. Method Description

We will now particularize the DoE flow for the case of a DC-DC Buck converter. The proposed approach consists of the following steps:

a) *Determine the nominal values for the PID*

A first preliminary step is to determine a nominal set of PID parameters around which the experiments are done. For this purpose, the PID tuning was done using a pole-placement technique in the *z*-domain, such that specific time-domain constraints are achieved, *i.e.* overshoot smaller than 10% and settling time smaller than 250us. Moreover, the limit cycles conditions suppression were checked and satisfied by the current chosen PID values (Amariutei *et al.*, 2015b): K_p = 46.9; K_i = 2.8; K_d = 428.03. These PID values satisfy the imposed constraints for the test scenarios of interest: input step scenario (from 8 V to 12 V at high load current) and load step scenario (from 311.2 mA to 11.2 mA at 8 V input voltage).

b) *Plan the experiments*

As previously mentioned, the inputs for the experiments are the three PID parameters, namely: K_p , K_i and K_d. These parameters are varied within a range of ±20% from the nominal set of values determined in previous step. Each variation range is divided in 11 intervals and a full grid experiment is used, *i.e.*, a number of 1331 different PID sets should be simulated.

c) *Run simulations and gather useful information*

For each PID set of coefficients within the experiment, a simulation is done using the nonlinear model of the DC-DC Buck converter. After each run, the overshoot and the settling time are extracted from the time-domain waveform of the output voltage and are saved for further processing. These values will be therefore used for fitting the experimental data to a mathematical model.

d) *Identify the mathematical expression used for estimating the overshoot and settling time performances*

The mathematical model that is used for estimating the time-domain performances is based on a multi-variable FFT. The overshoot and the settling time are expressed as functions of the three PID parameters as:

$$\widehat{Ovsh}(n,m,p)=\frac{1}{NMP}\sum_{k=1}^{N}\sum_{l=1}^{M}\sum_{q=1}^{P}FFT\big(Ovsh(k,l,q)\big)\,f_{\exp}(n,m,p), \qquad (2)$$

$$\widehat{SettTime}(n,m,p)=\frac{1}{NMP}\sum_{k=1}^{N}\sum_{l=1}^{M}\sum_{q=1}^{P}FFT\big(SettTime(k,l,q)\big)\,f_{\exp}(n,m,p), \qquad (3)$$

$$f_{\exp}(n,m,p) = \mathrm{e}^{\mathrm{j}2\pi\left(\frac{(k-1)(n-1)}{N}+\frac{(l-1)(m-1)}{M}+\frac{(q-1)(p-1)}{P}\right)}, \quad (4)$$

where: *N, M, P* represents the number of levels chosen for each PID dimension (in this case 11), *Ovsh*(*k,l,q*), *SettTime*(*k,l,q*) are the results extracted from the time-domain simulation, and $\widehat{Osvh}(n,m,p)$, $\widehat{SettTime}(n,m,p)$ are the calculated estimates using the FFT.

From (2)-(4), it can be observed that the number of Fourier coefficients used in the approximation equals the total number of performed simulations, particularly 1331 simulations. However, several conditions regarding the magnitude of the frequency components can be imposed such that some of the FFT coefficients can be filtered out without significantly affecting the accuracy.

e) *Determine the approximation errors*

As previously mentioned, a validation step is required to determine the accuracy of the obtained estimation. For this purpose, the 2-norm distance is used:

$$Err_{Ovsh} = \sqrt{\frac{1}{NMP}\sum_{k=1}^{N}\sum_{l=1}^{M}\sum_{q=1}^{P}\left(\widehat{Ovsh}(k,l,q) - Ovsh(k,l,q)\right)}, \quad (5)$$

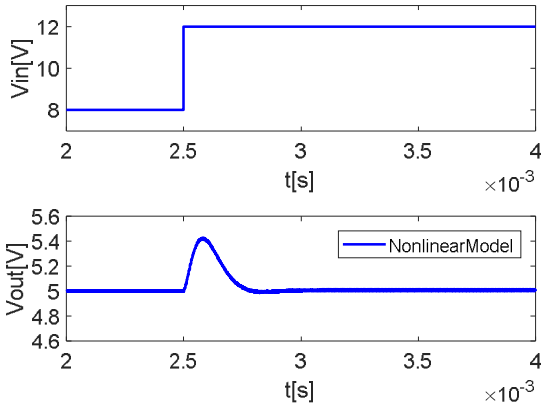
$$Err_{SettTime} = \sqrt{\frac{1}{NMP}\sum_{k=1}^{N}\sum_{l=1}^{M}\sum_{q=1}^{P}\left(\widehat{SettTime}(k,l,q) - SettTime(k,l,q)\right)}. \quad (6)$$

5. Simulation Results

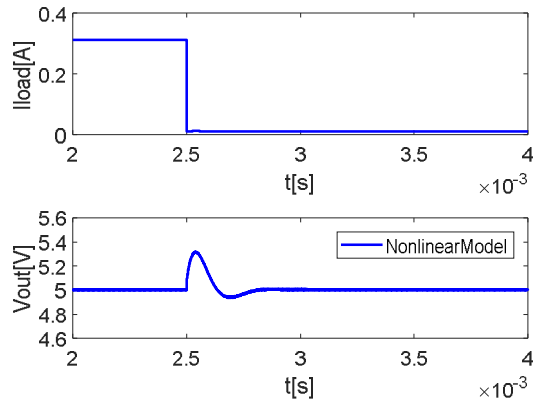
The above steps are applied on the Buck converter, running a total number of 1,331 simulations. As already mention, the two test scenarios are considered of interest are: an input step from 8 V to 13 V with constant load current of 11.2 mA and load step from 11.2 mA to 311.2 mA at a constant input voltage of 8 V. The time-domain waveforms for the output voltage for the two test scenarios of interest using the nominal PID set are presented in Fig. 4.

In the following, a full-factorial experiment with 11 levels is built around the nominal PID set. The values of the controller (K_p , K_i , K_d) are varied within a tolerance of ±20%. Fig. 5 shows the sets of PID values used to build the full-factorial experiment and it highlights the nominal PID set.

For each of these PID pairs, time-domain simulations are performed on the nonlinear model and the overshoot and settling time values are automatically extracted. The obtained performances are shown in Fig. 6. This figure contains on one hand the results from all simulation runs, and on the other hand the surface representing the imposed time-domain specifications.



a) Input step



b) Load Step

Fig. 4 – Time domain performances – Nominal PID Set.

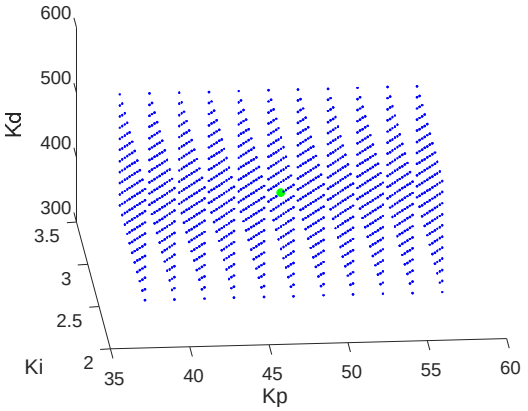
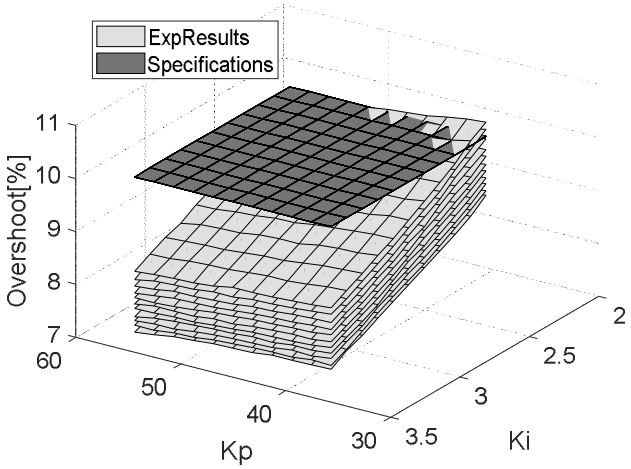
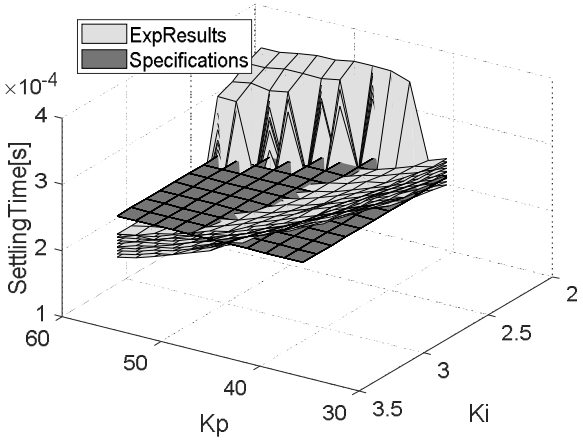


Fig. 5 – PID parameter variation.



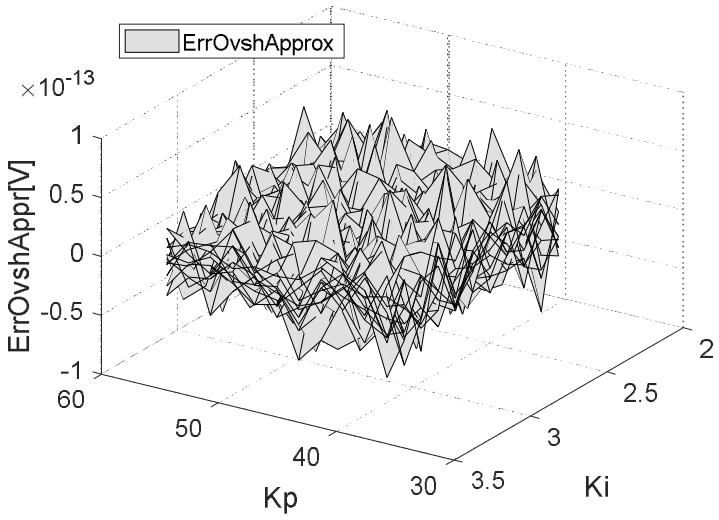
a) Overshoot values



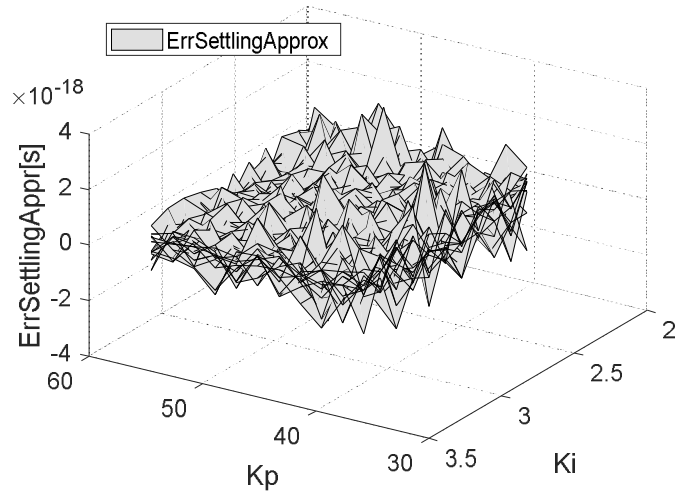
b) Settling time values

Fig. 6 – Input Step – time domain performances.

From the above plots, it can be observed that there is a limited area in which the PID sets can be varied such that the overshoot and the settling time remain beneath their maximum allowed values. If an accurate approximation of these surfaces could be extracted, then the values of the time-domain performances could be predicted without the need of further simulations. For this, the FFT is used. Using this approximation, a mathematical expression in K_p , K_i , K_d is deduced. The total number of coefficients present in the mathematical model equals the number of simulations, in this case 1331. The obtained errors between the FFT approximation and the simulation results are presented in Fig. 7.



a) Overshoot approximation errors

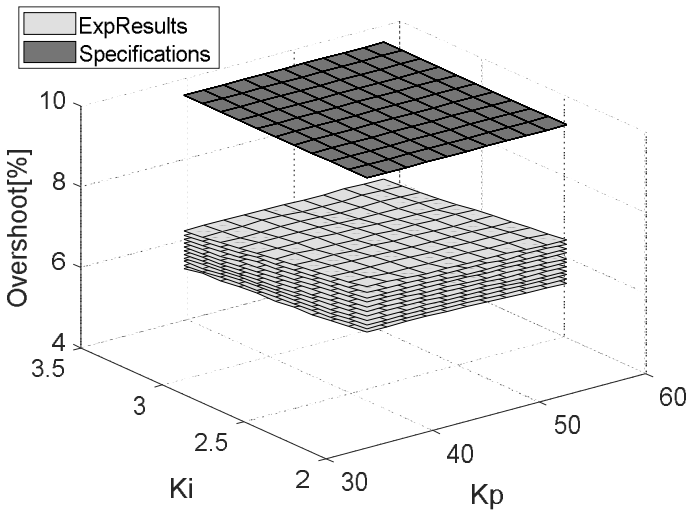


b) Settling time approximation error

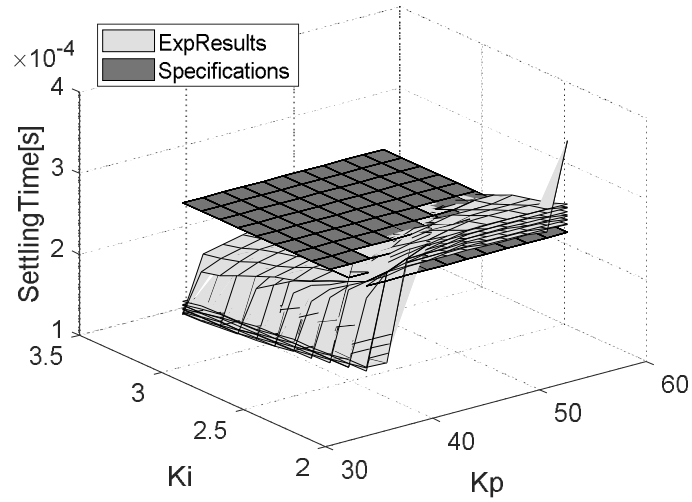
Fig. 7 – Input Step – Approximation errors.

From Fig. 7, it can be noticed that the errors coming from the FFT approximation are very small. The maximum error for the overshoot is $6.75e^{-14}$, while the maximum error for the settling time is $2.818e^{-18}$. *Hence, the calculated Fourier coefficients can be used to predict the values of the time-domain performances for any PID set inside the ±20% tolerance range.*

The results from the full-factorial experiment on the load step scenario are shown in Fig. 8.



a) Overshoot values



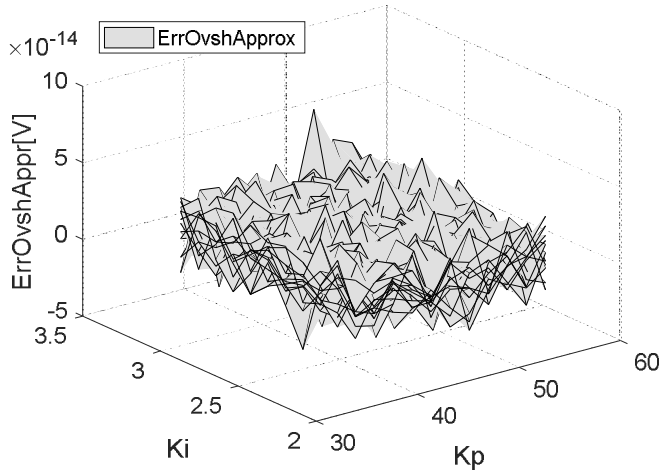
b) Settling Time Values

Fig. 8 – Load Step – Time domain performances.

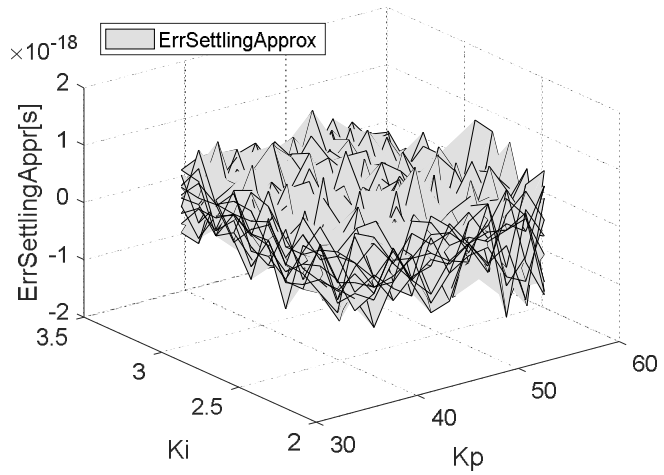
In the case of load step scenario, the overshoot specification is met in the entire range of parameter variation, while for the settling time there is one area in which the obtained values are above the allowed value.

It can be observed that, for both test scenarios, the overshoot surface is smooth, while the settling time surface has many local extreme values. The value of the settling time is strongly influenced by the presence of limit cycles on the output voltage.

The approximation errors for the load step case are shown in Fig. 9.



a) Overshoot approximation errors



b – Settling time approximation error

Fig. 9 – Load Step – Approximation Errors.

The approximation errors are again very small. The maximum error for the overshoot reaches a value of $5.5e^{-14}$, while for the settling time the maximum value is $1.192e^{-18}$.

6. Conclusion

The brute force way to determine the performances of a converter when changing the PID parameters would be to make a new simulation/measurement

for every set of parameters that should be tested. Therefore, the simulation time increases with the number of PID sets to be checked. The aim is to obtain a mathematical model as in (1) which is usually done through polynomial approximation. It has been shown that in comparison to the polynomial approximation, the proposed method based on three-dimensional FFT offers better accuracy. However, if the constrains for the error are relaxed, a much lower number of Fourier coefficients can be used to analytically describe the mathematical form of the DoE.

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ESTIMAREA PERFORMANTELOR UNUI CONVERTOR CC-CC DE TIP BUCK PRIN INTERMEDIUL METODEI DE PLANIFICARE A EXPERIMENTELOR

(Rezumat)

Planificarea experimentelor este un concept care este de cele mai multe ori utilizat in abordări de tip “cutii negre” sau “cutii gri” din care ieşirile de interes ale sistemului sunt dificil de exprimat prin intermediul unor expresii matematice. Această lucrare prezintă modul în care metoda de planificare a experimentelor poate fi utilizată pentru a estima performanţele din domeniul timp (supracreşterea şi timpul de stabilizare) pentru un convertor CC-CC de tip Buck. Contrar abordării polinomiale, în acest articol este utilizată o funcţie de estimare bazată pe FFT. Aceasta oferă un compromis mai bun între numărul de experimente necesare şi acurateţea obţinută. Rezultatele prezentate pe parcursul lucrării sunt bazate pe simulări Matlab. Pentru a valida valorile estimate prin FFT, pe parcursul articolului sunt prezentate diverse simulări în domeniul timp. Metoda propusă poate fi aplicată atât direct pe masurători cât şi pe simulări (aşa cum s-a prezentat în cazul de faţă).