BULETINUL INSTITUTULUI POLITEHNIC DIN IAŞI
Publicat de
Universitatea Tehnică „Gheorghe Asachi” din Iaşi
Volumul 64 (68), Numărul 3, 2018
Secția
ELECTROTEHNICĂ. ENERGETICĂ. ELECTRONICĂ

A NOTE ON MODELLING APPROACHES FOR A DC-DC BUCK CONVERTER WITH SOFTWARE CONTROL LOOP

BY

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Received: July 20, 2018
Accepted for publication: August 29, 2018

Abstract. Developing high-performance DC-DC converter applications usually involves building accurate simulation models that can be used for appropriate tuning of the control loop. The present work focuses on investigating various models built for a DC-DC Buck converter controlled through a software PID routine. Since the control is done in software, the application should cope with both analog and digital models and signals. Using appropriate conversion techniques, the option of building all analog or all digital linearized models arises. To find the best option, two linearized models, a pure analog model and a pure digital model, are compared with the linear and nonlinear mixed analog-digital models. The comparison is done based on time-domain responses for two test scenarios of interest: input and load steps. The conclusion of the Matlab simulation results presented throughout the paper is that a pure digital linearized model presents a better behaviour of the output voltage than the pure analog one.

Key words: DC-DC Buck converter; Linearized Models; ZOH transform.

1. Introduction

This work presents several modelling choices for a DC-DC Buck converter. This kind of application aims at obtaining a stable output voltage

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regardless of input or load current disturbances that can appear during the normal operation of the system. To achieve this goal, several tuning methods were developed throughout the years. The control parameters can be tuned either using trial-and-errors methods (Astrom & Hagglund, 2004) or using analytical methods (Abe *et al.*, 2011; Garpinger & Hagglund, 2008; Kurokawa *et. al.*, 2010; Shahroki & Zomorrodi, 2012; Zhang *et. al.*, 2002). Many of the existing tuning methods require linear/linearized models for the application under study. Therefore, a preliminary step for tuning the control parameters is to build and use accurate linearized models for the time-domain behaviour of the converter.

The paper is organized as follows. Section **2** covers general aspects regarding the DC-DC Buck converter under study and Section **3** presents in detail the steps that are done to build several linearized models for the application. Comparison between the various models is done in Section **4** based on the transient responses for two scenarios of interest: step on input voltage and step on load current. Section **5** draws the conclusions on the modelling choices for a DC-DC Buck converter.

2. Application Overview

The following considerations are focused on a DC-DC Buck converter using a software control loop as shown in Fig. 1.

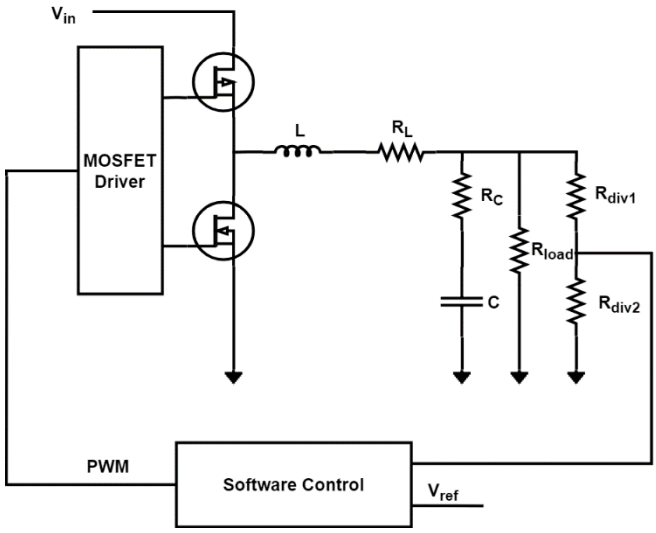

Fig. 1 – DC-DC Buck Converter – Block Diagram.

As it can be seen the application under study works with both analog and digital signals. The analog part of the converter consists of a half-bridge configuration and an LC output filter, while the digital part comprises of a

micro-controller responsible for the control mechanism. The output voltage of the converter is read into an ADC block via a resistor divider, and the obtained digital value is compared with the equivalent digital value of a fixed 5V reference voltage. A PID algorithm is implemented in software, with its parameters chosen such as good transient performances for the DC-DC converter are obtained. The behaviour of the Buck converter is investigated in the following two scenarios: load steps and input steps.

3. Modelling Levels

The target of the application under study is to deliver a constant output voltage even when the system is affected by disturbances (input voltage and load current). Thus, several time-domain performances such as overshoot and settling time are imposed to limit the negative effects that the converter could produce on the systems that are supplied from it. The desired performances can be achieved by a good tuning of the control loop. In what follows, several linearized models are presented, and their transient responses are compared with the ones obtained after simulating the nonlinear model. Therefore, the nonlinear model is taken as the reference model and it is desired that the responses of the linearized models are as close as possible to the ones obtained via this nonlinear simulation.

3.1. Nonlinear Model

The nonlinear model for the DC-DC Buck Converter is done using the Simscape Matlab Toolbox. Using this approach, the analog part of the converter is built using the available models for the electrical components, while the control is modelled through digital transfer functions as shown in Fig. 2.

Since in conduction, the MOSFETs of the half-bridge configuration (M1 and M2) work in the triode region, they are modelled as real switches characterized by a resistance in ON state with r_{ds_on} value. The model for the LC output filter considers the parasitic series resistances of the inductor (R_L) and of the capacitor (R_C). The load of the DC-DC converter is purely resistive (R_{Load}). In order to apply load step scenarios, an additional resistor is connected through a switch to R_{Load}. In this way, different load current steps can be modelled.
The software control loop is implemented with the use of a micro-controller. Hence, the sub-blocks needed to be modelled are: the 12 bits ADC, the PID routine, the inherent delay and the PWM generator.

The ADC block is modelled by its gain (1) and a quantization block:

$$K_{\mathrm{ADC}} = \frac{2^{N_{\mathrm{ADC}}} - 1}{V_{\mathrm{ADC\_ref}}}, \tag{1}$$

where: N_{ADC} – represents the resolution of the ADC block (12 bits) and $V_{\mathrm{ADC\_ref}}$ – is the reference voltage for the ADC converter (3.3V). A resistor divider is

added at the output voltage of the converter to adjust the voltage level to the allowed value of 3.3V.

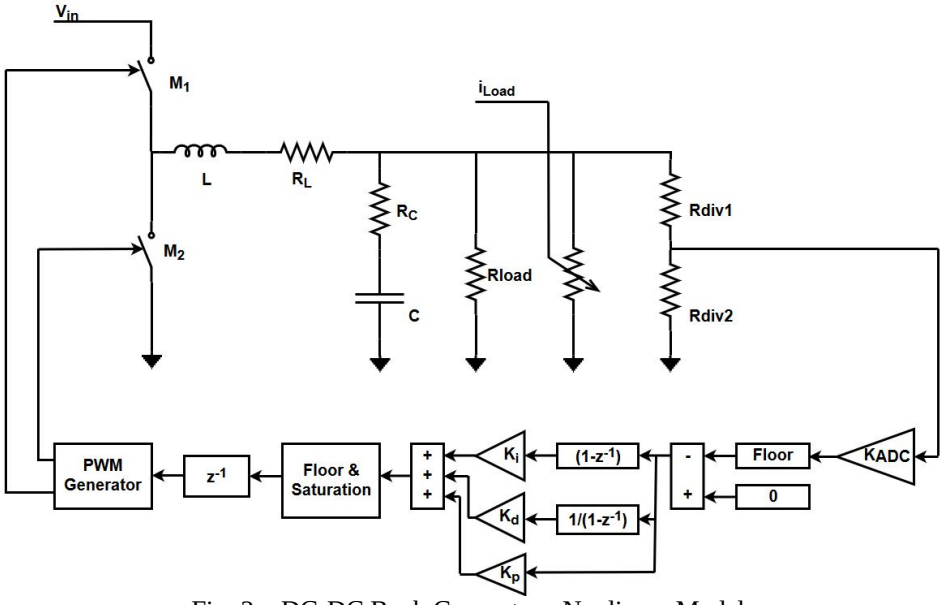

Fig. 2 – DC-DC Buck Converter - Nonlinear Model.

The PID controller is modelled using a parallel configuration of the discrete transfer function (2):

$$H_{\mathrm{PID}}(z) = K_p + K_i \frac{1}{1-z^{-1}} + K_d(1-z^{-1}), \tag{2}$$

where: K_p, K_i and K_d are the control parameters (real positive numbers). The role of the PID block is to minimize the error between the output voltage of the converter and the reference voltage by adjusting the duty cycle of the PWM signal applied to the MOSFETs. Since the PWM signals are internally generated by the micro-controller, only integer values for duty cycle are allowed, therefore a rounding block (floor) is added at the output of the PID block. Moreover, since the duty cycle is limited to the range between 0 and a maximum value of the PWM period register that depends on the desired PWM frequency, a saturation block is also added.

3.2. Linearized Mixed Analog-Digital Model

In order to obtain the linearized model for the Buck converter, both the analog and the digital parts have to be linearized. For the discrete part, the linearization is simply done by removing the quantization and saturation blocks, while for the analog part the linearization is done using the generic approach

presented in (Erickson & Maksimovic, 2004). The analog part is therefore analysed by writing down the state-equations valid for the two cases: one when the high-side MOSFET is ON and the second case when the low-side MOSFET is ON.

When the PWM signal is active (during the T_{on} interval the high-side MOSFET is ON), the equivalent circuit for the analog part is given in Fig. 3.

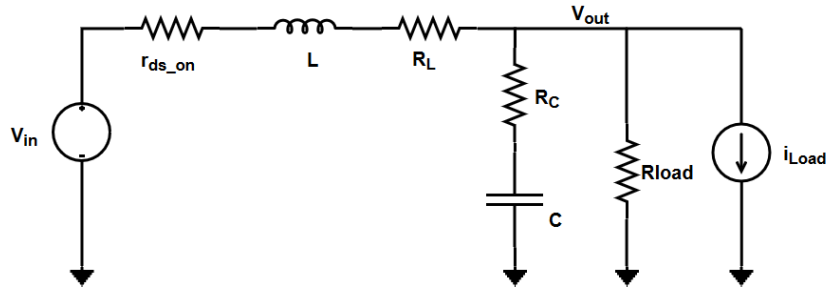

Fig. 3 – Equivalent circuit valid for T_{on}.

The state equations valid in this case are given:

$$\begin{cases} \dfrac{\mathrm{d}i_L(t)}{\mathrm{d}t} = \dfrac{1}{L}\Big[v_{\text{in}}(t) - i_L(t)\big(r_{\text{ds\_on}} + R_L\big) - v_{\text{out}}(t)\Big], \\ \dfrac{\mathrm{d}v_C(t)}{\mathrm{d}t} = \dfrac{1}{R_{\text{load}}C}\big[i_L(t)R_{\text{load}} - v_{\text{out}}(t) - i_{\text{load}}(t)R_{\text{load}}\big], \\ v_{\text{out}}(t) = v_C(t) + C\dfrac{\mathrm{d}v_C(t)}{\mathrm{d}t}R_C. \end{cases} \tag{3}$$

The equivalent circuit valid for T_{off} (low-side MOSFET is ON) is shown in Fig. 4.

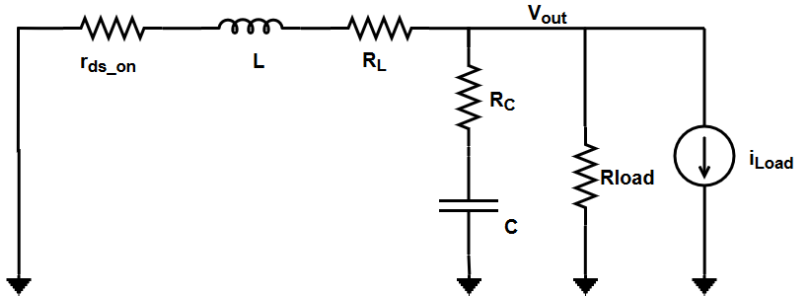

Fig. 4 – Equivalent circuit valid for T_{off}.

Hence, for the case when the PWM signal is OFF, the state equations are:

$$\begin{cases} \dfrac{\mathrm{d}i_L(t)}{\mathrm{d}t} = \dfrac{1}{L}\Big[-i_L(t)\big(r_{\mathrm{ds\_on}} + R_L\big) - v_{\mathrm{out}}(t)\Big], \\ \dfrac{\mathrm{d}v_C(t)}{\mathrm{d}t} = \dfrac{1}{R_{\mathrm{load}}C}\big[i_L(t)R_{\mathrm{load}} - v_{\mathrm{out}}(t) - i_{\mathrm{load}}(t)R_{\mathrm{load}}\big], \\ v_{\mathrm{out}}(t) = v_C(t) + C\dfrac{\mathrm{d}v_C(t)}{\mathrm{d}t}R_C. \end{cases} \tag{4}$$

After averaging the behaviour of the converter given in Eqs. (3) and (4) over a PWM period, the following set of equations is obtained:

$$\begin{cases} \dfrac{\mathrm{d}\langle i_L(t)\rangle_{T_{\mathrm{pwm}}}}{\mathrm{d}t} = \mathrm{d}(t)\dfrac{1}{L}v_{\mathrm{in}}(t) + \dfrac{1}{L}\Big[-i_L(t)\big(r_{\mathrm{ds\_on}} + R_L\big) - v_{\mathrm{out}}(t)\Big], \\ \dfrac{\mathrm{d}\langle v_C(t)\rangle_{T_{\mathrm{pwm}}}}{\mathrm{d}t} = \dfrac{1}{R_{\mathrm{load}}C}\big[i_L(t)R_{\mathrm{load}} - v_{\mathrm{out}}(t) - i_{\mathrm{load}}(t)R_{\mathrm{load}}\big], \\ \langle v_{\mathrm{out}}(t)\rangle_{T_{\mathrm{pwm}}} = \langle v_C(t)\rangle_{T_{\mathrm{pwm}}} + CR_C\dfrac{\mathrm{d}\langle v_C(t)\rangle_{T_{\mathrm{pwm}}}}{\mathrm{d}t}. \end{cases} \tag{5}$$

From Eq. (5) two sets of equations can be derived: one that describes the steady state behaviour of the system and one that describes the dynamic behaviour of the system when several disturbances are applied at its inputs. The equations that characterize the DC-DC Buck converter in steady state are:

$$\begin{cases} I_L = \dfrac{V_{\mathrm{in}}D}{R_{\mathrm{load}} + r_{\mathrm{ds\_on}} + R_L}, \\ V_C = \dfrac{V_{\mathrm{in}}DR_{\mathrm{load}}}{R_{\mathrm{load}} + r_{\mathrm{ds\_on}} + R_L}, \\ V_{\mathrm{out}}(t) = V_C = \dfrac{V_{\mathrm{in}}DR_{\mathrm{load}}}{R_{\mathrm{load}} + r_{\mathrm{ds\_on}} + R_L}. \end{cases} \tag{6}$$

The dynamics of the converter are described by the following system of equations:

$$\begin{cases} \dfrac{\mathrm{d}\langle \widehat{i_L(t)}\rangle_{T_{\mathrm{pwm}}}}{\mathrm{d}t} = \dfrac{V_{\mathrm{in}}\widehat{\mathrm{d}(t)} + D\widehat{v_{\mathrm{in}}(t)} - \big(r_{\mathrm{ds\_on}} + R_L\big)\widehat{i_L(t)} - \widehat{v_{\mathrm{out}}(t)}}{L}, \\ \dfrac{\mathrm{d}\langle \widehat{v_C(t)}\rangle_{T_{\mathrm{pwm}}}}{\mathrm{d}t} = \dfrac{1}{R_{\mathrm{load}}C}\Big[R_{\mathrm{load}}\widehat{i_L(t)} - \widehat{v_{\mathrm{out}}(t)} - R_{\mathrm{load}}\widehat{i_{\mathrm{load}}(t)}\Big], \\ \langle \widehat{v_{\mathrm{out}}(t)}\rangle_{T_{\mathrm{pwm}}} = \langle \widehat{v_C(t)}\rangle_{T_{\mathrm{pwm}}} + CR_C\dfrac{\mathrm{d}\langle \widehat{v_C(t)}\rangle_{T_{\mathrm{pwm}}}}{\mathrm{d}t}. \end{cases} \tag{7}$$

Applying the Laplace transform for the system of Eqs. (7), the s-domain transfer functions of interest can be determined:

– Transfer Function from input voltage to output:

$$H_{\text{in\_out}}(s)=\frac{H_{\text{in\_out\_0}}\left(1-s/\omega_{z1}\right)}{\left(s/\omega_0\right)^2+s/Q\omega_0+1}; \tag{8}$$

– Transfer Function from PWM input (control input) to output:

$$H_{\text{ctrl\_out}}(s)=\frac{H_{\text{ctrl\_out\_0}}\left(1-s/\omega_{z1}\right)}{\left(s/\omega_0\right)^2+s/Q\omega_0+1}; \tag{9}$$

– Output impedance:

$$Z_{\text{out}}(s)=\frac{Z_{\text{out\_0}}\left(1-s/\omega_z\right)\left(1-s/\omega_{z1}\right)}{\left(s/\omega_0\right)^2+s/Q\omega_0+1}, \tag{10}$$

where the parameters used in the transfer functions depend on the values of the LC output filter, the load resistance and the $r_{\text{ds\_on}}$ value of the MOSFETs from the driver module. The expressions for the parameters can be found in (Amariuței *et al.*, 2015). Using the above transfer functions, the Linearized Mixed model can be implemented as shown in Fig. 5.

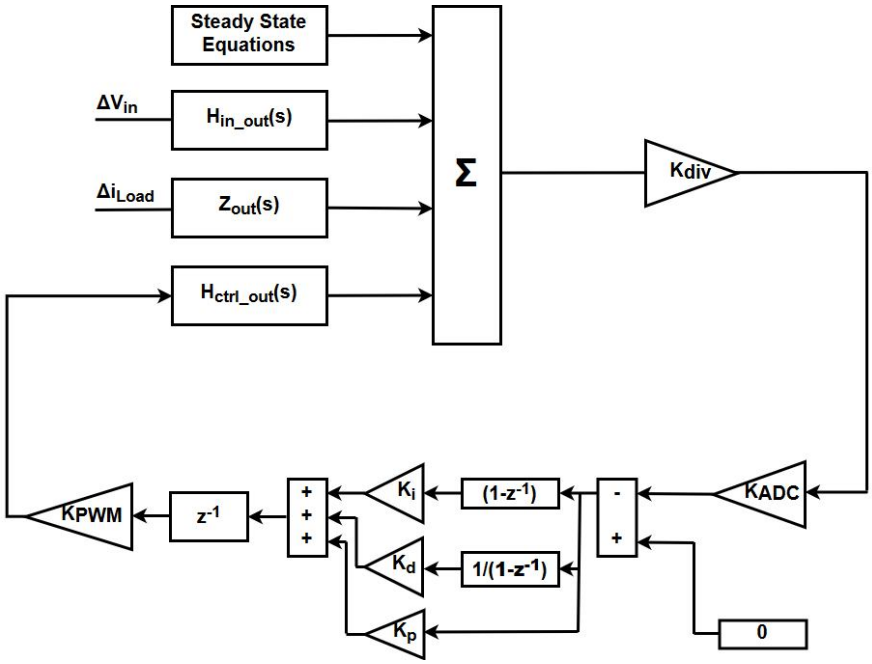

Fig. 5 – DC-DC Buck Converter - Linearized Mixed Model.

The Linearized Mixed model is useful for extracting simulation results as it offers the most accurate results, as it will be shown further on. Since it works both with analog and discrete signals, this model cannot be used for tuning the control loop by means of analytical expressions. Therefore, two alternatives of this model are additionally built: one using only analog signals and another one using only discrete signals.

3.3. Linearized Model using only Discrete Signals

To build the linearized model that works only with discrete signals, the s-domain transfer functions given in Eqs. (8),...,(10) should be transformed into the discrete domain. Since the perturbations are given as step inputs, the most appropriate analog-to-digital transformation is the ZOH (Zero-Order-Hold) also known as the step-invariant transform. This means that the step response of the original analog transfer function is identical to the one obtained by its discrete counterpart. For a generic *s*-domain transfer function H(s), the digital version obtained using the ZOH is determined using the expression:

$$H(z)=\left(1-z^{-1}\right)\boldsymbol{Z}\left\{Sampling\left[\boldsymbol{L}^{-1}\frac{H(s)}{s}\right]\right\}. \tag{11}$$

For the particular case of the DC-DC converter, the ZOH transform is applied for all of the three transfer functions of interest presented in Eqs. (8),...,(10). The equivalent discrete transfer functions have the following *z*-domain expressions:

– Transfer Function from input voltage to output:

$$H_{\text{in\_out\_ZOH}}(z)=\frac{H_{\text{in\_out\_ZOH\_0}}\left(a_{1\_\text{ZOH}}z+a_{0\_\text{ZOH}}\right)}{b_{2\_\text{ZOH}}z^2+b_{1\_\text{ZOH}}z+b_{0\_\text{ZOH}}}; \tag{12}$$

– Transfer Function from PWM input (control input) to output:

$$H_{\text{ctrl\_out\_ZOH}}(z)=\frac{H_{\text{ctrl\_out\_ZOH\_0}}\left(a_{1\_\text{ZOH}}z+a_{0\_\text{ZOH}}\right)}{b_{2\_\text{ZOH}}z^2+b_{1\_\text{ZOH}}z+b_{0\_\text{ZOH}}}; \tag{13}$$

– Output impedance:

$$Z_{\text{out\_ZOH}}(z)=\frac{Z_{\text{out\_ZOH\_0}}\left(c_{2\_\text{ZOH}}z^2+c_{1\_\text{ZOH}}z+c_{0\_\text{ZOH}}\right)}{b_{2\_\text{ZOH}}z^2+b_{1\_\text{ZOH}}z+b_{0\_\text{ZOH}}}, \tag{14}$$

where the expressions for the involved parameters are:

$$H_{\text{in\_out\_ZOH\_0}}=\frac{H_{\text{in\_out\_0}}}{\omega_{z1}\beta}; \tag{15}$$

$$H_{\text{ctrl\_out\_ZOH\_0}} = \frac{H_{\text{ctrl\_out\_0}}}{\omega_{z1}\beta}; \tag{16}$$

$$Z_{\text{out\_ZOH\_0}} = \frac{Z_{\text{out\_0}}}{\omega_{z1}\omega_z\beta}; \tag{17}$$

$$a_{1\_\text{ZOH}} = \left[-\delta\sin(\alpha) - \omega_{z1}\beta\cos(\alpha)\right]e^{\gamma} + \omega_{z1\beta}; \tag{18}$$

$$a_{0\_\text{ZOH}} = -\omega_{z1}\beta + e^{\gamma}\left[-\delta\sin(\alpha) - \omega_{z1}\beta\cos(\alpha)\right]; \tag{19}$$

$$b_{2\_\text{ZOH}} = 1; \tag{20}$$

$$b_{1\_\text{ZOH}} = -2\cos(\alpha)e^{\gamma}; \tag{21}$$

$$b_{0\_\text{ZOH}} = e^{2\gamma}; \tag{22}$$

$$c_{2\_\text{ZOH}} = \omega_0^2\beta; \tag{23}$$

$$c_{1\_\text{ZOH}} = \left[-\rho\sin(\alpha) + \left(\omega_0^2 - \omega_{z1}\omega_z\right)\beta\cos(\alpha)\right]e^{\gamma} - \omega_0^2\beta; \tag{24}$$

$$c_{0\_\text{ZOH}} = \left[\rho\sin(\alpha) + \left(\omega_0^2 - \omega_{z1}\omega_z\right)\beta\cos(\alpha)\right]e^{\gamma} + \omega_{z1}\omega_z\beta e^{2\gamma}; \tag{25}$$

$$\alpha = \frac{1}{2}\cdot\frac{\omega_0\sqrt{2Q-1}\sqrt{2Q+1}T_{pwm}}{Q}; \tag{26}$$

$$\beta = \sqrt{2Q-1}\sqrt{2Q+1}; \tag{27}$$

$$\gamma = \frac{1}{2}\cdot\frac{\omega_0 T_{pwm}}{Q}; \tag{28}$$

$$\delta = \omega_{z1} + 2\omega_0 Q; \tag{29}$$

$$\rho = \omega_0^2 + 2\omega_0 Q\omega_{z1} + \omega_{z1}\omega_z + 2\omega_0 Q\omega_z. \tag{30}$$

The Linearized Discrete Model shown in Fig. 6 is built replacing the s-domain transfer functions from Eqs. (8),...,(10) with their equivalent z-domain transfer functions given in Eqs. (12),...,(14), while the remaining blocks are unchanged:

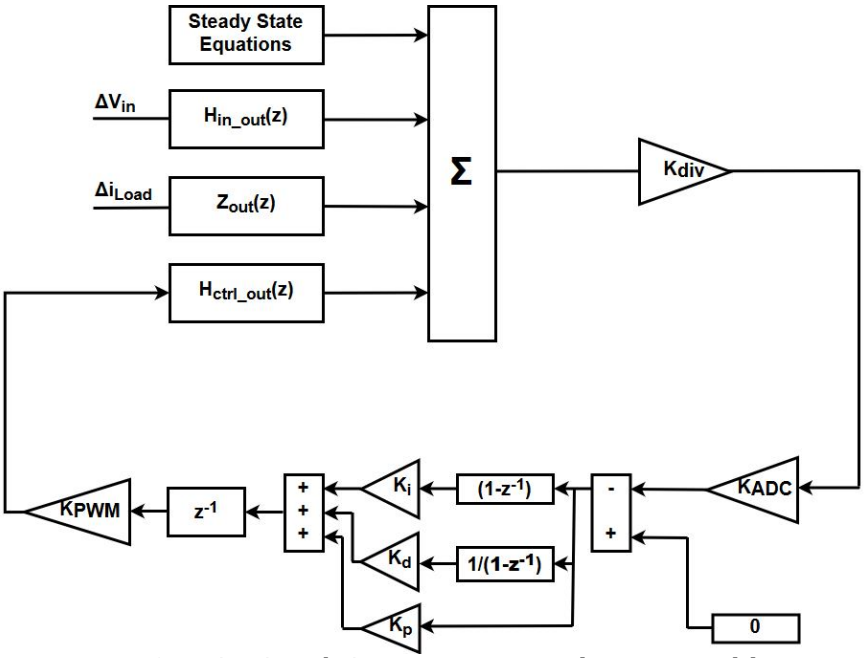

Fig. 6 – DC-DC Buck Converter - Linearized Discrete Model.

3.4. Linearized Model using only Analog Signals

For building the linearized analog model, the blocks that work with discrete signals should be converted into analog domain. For this, the inverse ZOH transform should be employed for the blocks from the feedback path, including the PID and the delay block. To be able to apply the inverse ZOH transform, the discrete transfer functions that are subject to the conversion must satisfy the following set of conditions:

a) the *z*-domain transfer function should not contain any negative real pole;

b) the *z*-domain transfer function should not contain poles at the origin (*i.e.* pure time-delays).

Since both the PID transfer function and the unit delay have poles at the origin, the inverse ZOH transform cannot be directly applied on these functions. Thus, a work-around is applied: the loop transfer function of the system is first determined in the *z*-domain and the inverse ZOH transform is applied on this resulted transfer function.

The *z*-domain loop transfer function expression can be expressed as:

$$T(z) = K_{sys} H_1(z) H_2(z), \tag{31}$$

where:

$$H_1(z) = z^{-2}, \tag{32}$$

$$H_2(z) = H_{\text{ctrl\_out}}(z) H_{\text{PID}}(z) z. \tag{33}$$

By using this approach, the transfer function $H_2(z)$ satisfies all conditions imposed by the inverse ZOH transform, while for the $H_1(z)$ its equivalent can be calculated either using the general substitution $z = e^{sT_{pwm}}$, or using the bilinear transform. The current approach is based on using the bilinear transformation. After applying the ZOH and the bilinear transform, the analog version of $T(z)$ is obtained. Moreover, the s-domain expressions for all the three closed loop transfer functions of interest are:

$$H_{\text{in\_out\_closedloop}}(s) = \frac{H_{\text{in\_out}}(s)}{1 + T(s)}; \tag{34}$$

$$H_{\text{ctrl\_out\_closedloop}}(s) = \frac{H_{\text{ctrl\_out}}(s)}{1 + T(s)}; \tag{35}$$

$$Z_{\text{out\_closedloop}}(s) = \frac{Z_{\text{out}}(s)}{1 + T(s)}. \tag{36}$$

Using the above analog versions of the transfer functions, the Linearized Analog Model is presented in Fig. 7.

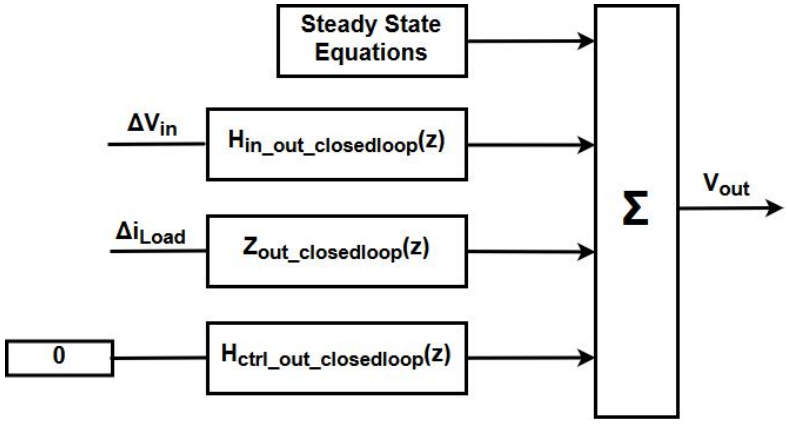

Fig. 7 – DC-DC Buck Converter - Linearized Analog Model.

4. Simulation Results

For each of the above models the transient behaviors in case of input and load current steps are presented. Four different test scenarios are

investigated: input Step from 8 V to 13 V with a constant load current of 312 mA; input Step from 13 V to 8 V with a constant load current of 312 mA; load current step from 312 mA to 12 mA with a constant input voltage of 8 V; load current step from 12 mA to 312 mA with a constant input voltage of 8 V.

All these scenarios are tested for three different PWM frequencies: 200 kHz, 100 kHz and 66 kHz.

4.1. Simulation Results for Input Step from 8V to 13V with Constant Load Current of 312mA

The simulation results for all four models working at a PWM frequency of 200 kHz in the case of an input step voltage from 8 V to 13 V are presented in Fig. 8. When the PWM frequency is changed to 100 kHz, the dynamics of the system look like that in Fig. 9, and for a PWM frequency of 66 kHz the results are shown in Fig. 10.

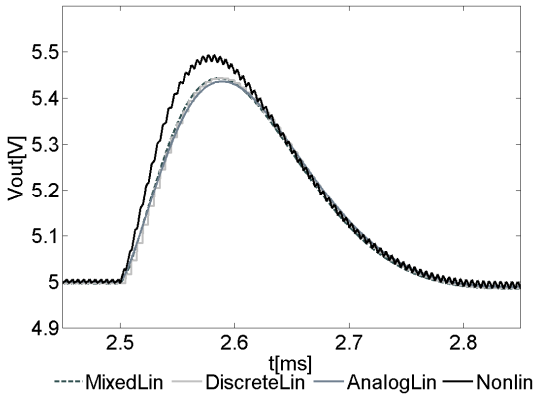

Fig. 8 – Input Step from 8V to 13V – 200kHz PWM frequency.

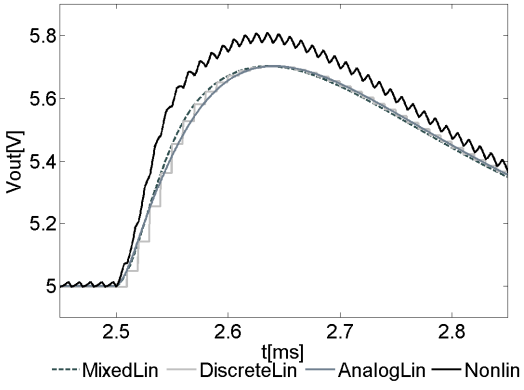

Fig. 9 – Input Step from 8V to 13V – 100kHz PWM frequency.

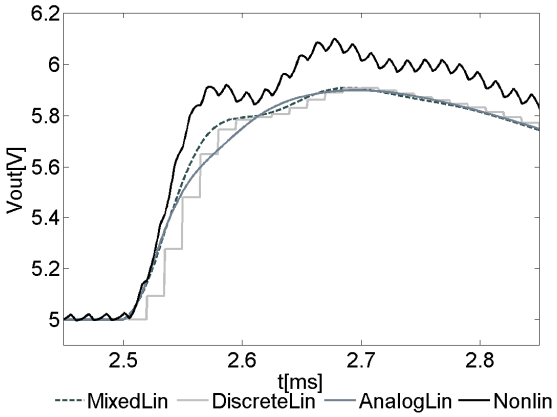

Fig. 10 – Input Step from 8V to 13V – 66kHz PWM frequency.

For relative high PWM frequencies (200kHz and 100kHz), the three linearized models produce similar transient responses. When the PWM frequency is lowered to 66kHz, only the linearized mixed and linearized pure discrete model can predict a similar dynamic behaviour as the one of the nonlinear model.

4.2. Simulation Results for Input Step from 13V to 8V with Constant Load Current of 312mA

The following figures present the dynamics of the output voltages exhibited by each of the four investigated models in case of applying input steps from 13 V to 8 V. The results are presented for three different PWM frequencies: as shown in Figs. 11,…,13.

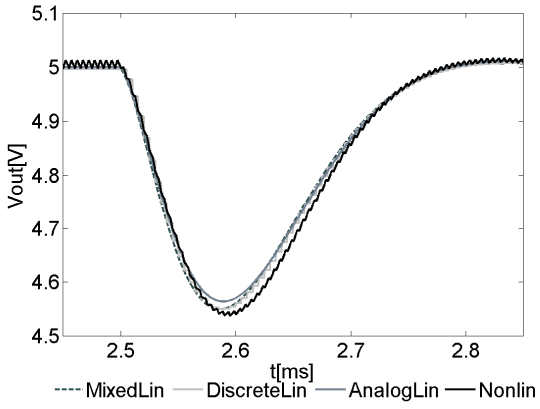

Fig. 11 – Input Step from 13V to 8V – 200kHz PWM frequency.

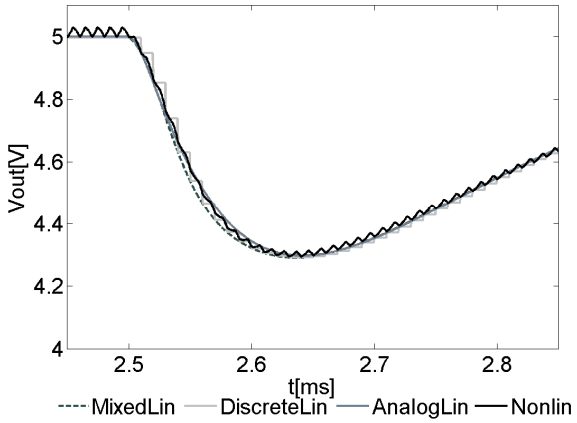

Fig. 12 – Input Step from 13V to 8V – 100kHz PWM frequency.

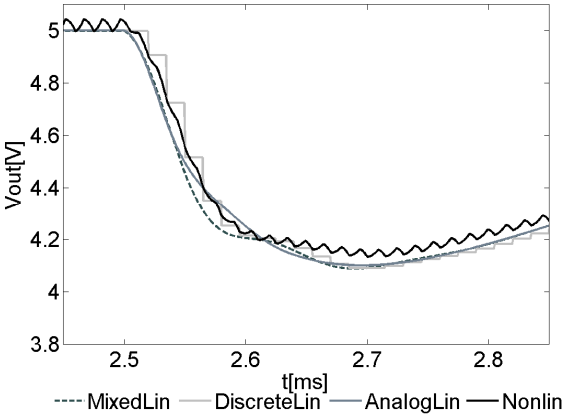

Fig. 13 – Input Step from 13V to
8V – 66kHz PWM frequency.

In this case the differences between the dynamics are very small, so all the models would predict the behavior of the output voltage with small error.

4.3. Simulation Results for Load Step from 12 mA to 312 mA with Constant Input Voltage of 8 V

The next test scenario of interest is the load step from low values to high values of load current. The output voltages computed with each of the four investigated models in this case are presented in Fig. 14 for 200 kHz PWM frequency, Fig. 15 for 100 kHz PWM frequency and Fig. 16 for 66 kHz PWM frequency.

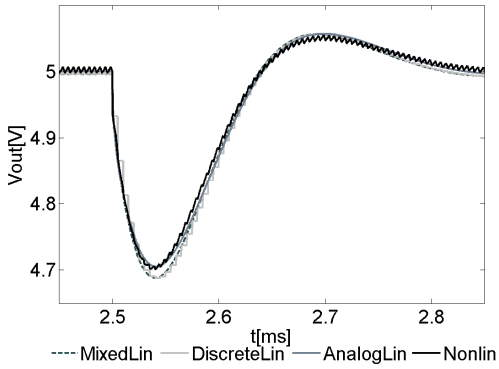

Fig. 14– Load Step from 12 mA to 312 mA – 200 kHz PWM frequency.

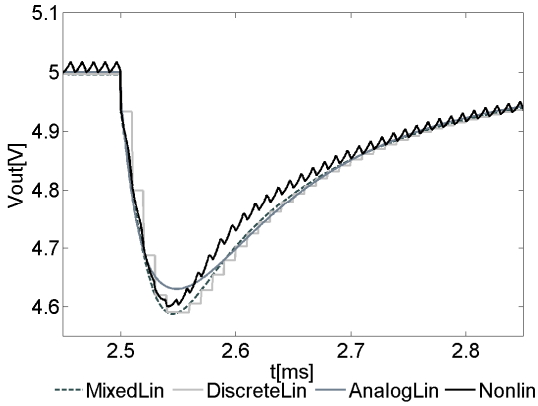

Fig. 15 – Load Step from 12 mA to 312 mA – 100 kHz PWM frequency.

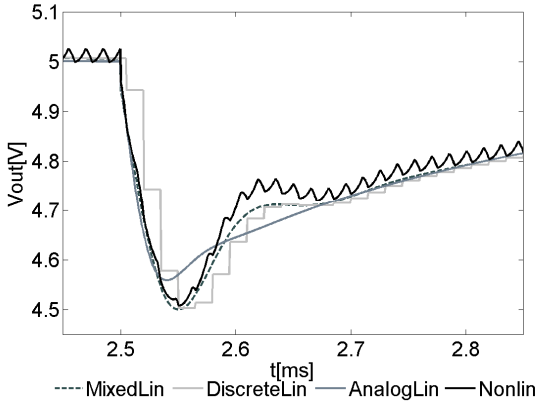

Fig. 16 – Load Step from 12mA to 312mA - 66kHz PWM frequency.

From the above results it can be concluded that the linearized model that works only with discrete signals can accurately predict the behavior of the output voltage of the DC-DC Buck converter. For relative high frequency, also the pure analog version of the model can be used, but if the PWM frequency is reduced than the error in predicting the dynamics of the output voltage using this model is higher.

4.3. Simulation Results for Load Step from 312mA to 12mA with Constant Input Voltage of 8V

Load step from high load currents to low currents has been investigated as well. The output voltages for the same three PWM frequencies are presented in Fig. 17 (200 kHz PWM frequency), Fig. 18 (100 kHz PWM frequency) and Fig. 19 (66 kHz PWM frequency).

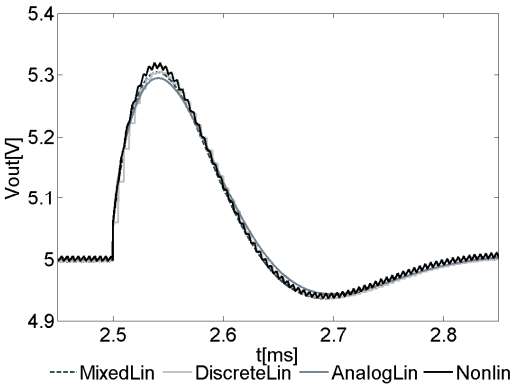

Fig. 17 – Load Step from 312 mA to 12 mA – 200 kHz PWM frequency.

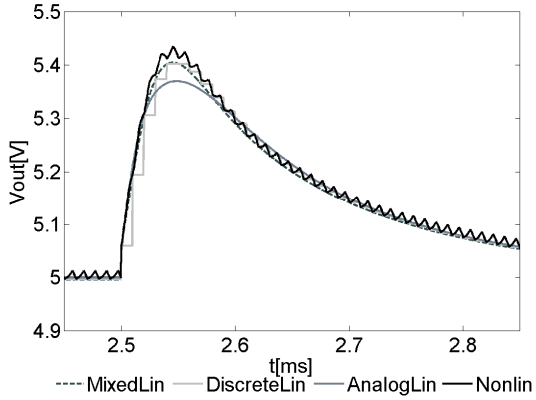

Fig. 18 – Load Step from 12 mA to 312 mA – 100 kHz PWM frequency.

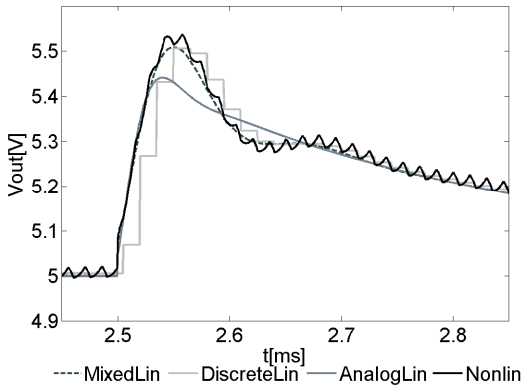

Fig. 19 – Load Step from 12 mA to 312 mA – 66 kHz PWM frequency

As in previous case, the linearized pure discrete model predicts with very good accuracy the dynamics of the output voltage, while the pure analog model will exhibit a high error when the PWM frequency is below 200 kHz.

6. Conclusion

This work focused on investigating four different models for the DC-DC Buck Converter since many tuning methods are based on analytical expressions for the system models under study. Hence the necessity of building linearized models for the Buck converter. Three different linearized models were derived: linearized model that works with signals from both digital and analog domains, linearized model with pure analog signals and linearized model with pure discrete signals. For comparison, input and load step scenarios were investigated. Simulation results showed that the linearized model using pure discrete signals is the best choice for the case of a DC-DC Buck converter with software control loop, since it offers a good prediction for the dynamics of the output voltage for all test scenarios and all the PWM frequencies investigated.

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ASUPRA MODELĂRII UNUI CONVERTOR CC-CC DE TIP BUCK CU BUCLĂ DE CONTROL SOFTWARE

(Rezumat)

Dezvoltarea convertoarelor de tip CC-CC de înaltă performanță implică, de obicei, construirea unor modele precise de simulare care să poată fi mai departe utilizate pentru reglarea corespunzătoare a buclelor de control. Lucrarea de față se axează pe investigarea diverselor modele construite pentru un convertor de CC-CC de tip Buck controlat printr-o rutină software PID. Aplicația de față lucrează atât cu semnale analogice cât şi cu semnale digitale. În total patru modele pentru convertorul de tip Buck sunt investigate: un model neliniar, un model linearizat care lucreaza şi cu semnale analogice şi cu semnale digitale, un model linearizat care lucrează doar cu semnale analogice şi un model linearizat care lucrează doar cu semnale digitale. Comparația îintre diversele modele se realizează pe baza comportării tranzitorii a tensiunii de la ieşirea convertorului. Patru scenarii de test sunt considerate: două de tip salt pe tensiunea de intrare şi două de tip salt pe curentul de sarcină. Rezultatele simulărilor Matlab prezentate pe parcursul acestei lucrări arată că un model linearizat pur discret oferă un comportament mai adecvat decât cel linearizat pur analogic.