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RECTIFIERS ENSURING HIGH EFFICIENCY IN UNITY POWER FACTOR CORRECTION APPLICATIONS

BY

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Abstract. The unity power factor correction rectifiers represent an ongoing research topic in the industry field. In this paper, six rectifier topologies claiming high efficiency, ensuring also a unity power factor correction (*e.g.* the six-switch, the SWISS, the eight-switch, the interleaved six-switch, the interleaved SWISS and the interleaved eight-switch rectifiers) are analyzed. The interleaved switching strategy implies a two-stage (interleaved) rectifier topology. This strategy cancels the AC-side input current harmonics and reduces the DC-side voltage ripples. The efficiency of the six unity power factor correction rectifiers is in here evaluated. The studies were performed in the simulation environment named GECKO Circuits. Accordingly, to the results obtained for the solutions employing the interleaved rectifier strategy topology are claiming higher power efficiency as compared with the single-stage topology ones.

Key words: rectifier; interleaved; efficient; unity power factor correction (PFC); harmonics.

1. Introduction

The power factor correction circuits have one major drawback, which is that they involve additional losses, and, the overall efficiency is reduced, then.

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In the literature, the SWISS rectifier, a buck-type third harmonic current injection rectifier, was first presented in (Soeiro, 2012) and it claims a 97% efficiency. Other recent publications report efficiencies of 98% for a unity power factor correction rectifier, namely the eight-switch from (Soeiro, 2013).

In this paper, new highly efficient unity power factor correction rectifier topologies are proposed. Some of them reach efficiency up to 98.7%. This is the case of the interleaved topologies of the six-switch, SWISS and eight-switch three-phase buck-type unity power factor correction rectifiers (Ancuți, 2015). These rectifiers are analysed using GECKO Circuits simulation environment. Then, the results are compared to each other in terms of efficiency and in the end, the conclusion are drawn.

2. Single-Stage Rectifier Topologies

In Fig. 1 the conventional six-switch unity power factor correction rectifier is presented.

Its control strategy, as depicted in Fig. 2, consists in two control loops: the outer control loop and the inner one (Fig. 2 *a*). The outer one is also the slower one of the two loops. It regulates the output voltage to a constant reference voltage u_{dc}^{*} and generates the reference value i_{dc}^{*}.

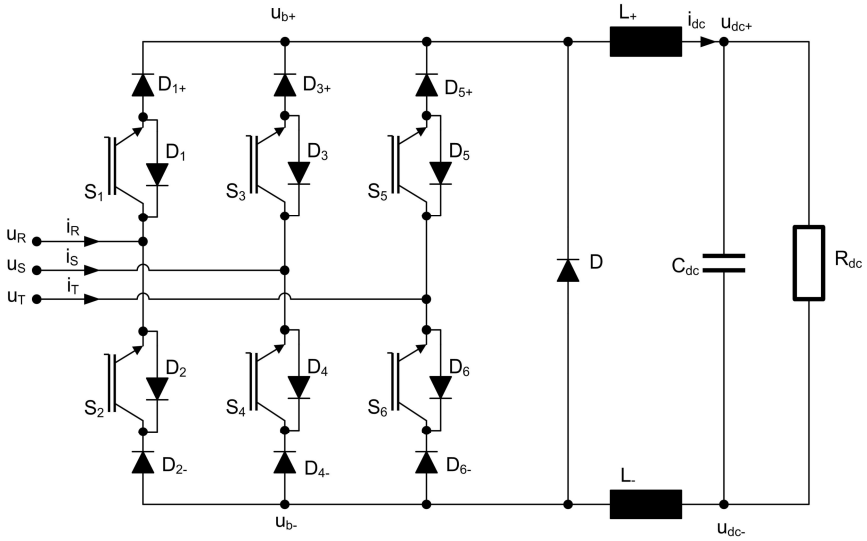


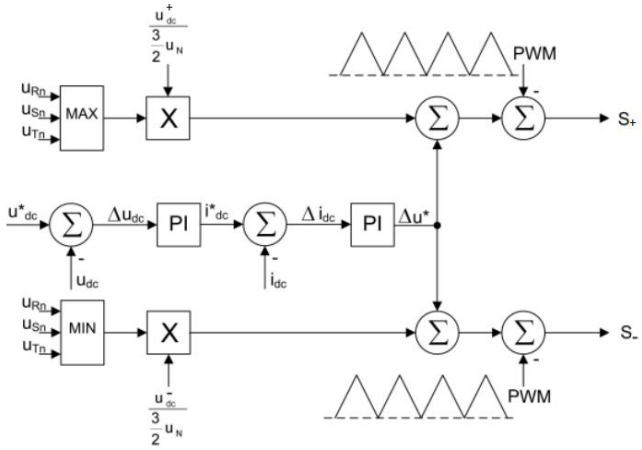
Fig. 1 − Six-switch rectifier topology scheme.

The inner loop is the fastest one and consists in a current controller that produces the output voltage reference value Δu^{*}, having as input the reference value i_{dc}^{*}, from which the measured dc inductor current is subtracted.

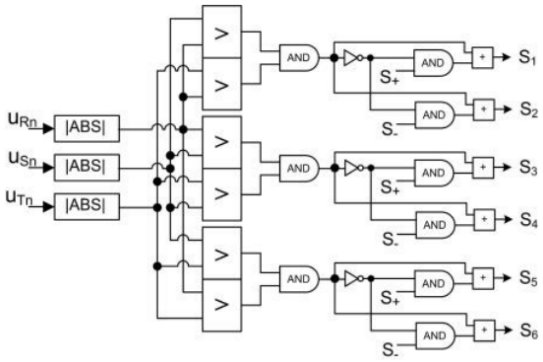
The positive and negative diode bridge output voltages (u_{dc}^{+} and $u_{dc}^{-)}$ and the output voltage reference u_N are then added as feed-forward loops to the

system reference value Δu^*. Then, by comparing the former resulting signals with a triangular carrier of 36 kHz, signals S_+ and S_- are generated.

From the rectifier input terminals, the signals u_{Rn}, u_{Sn}, u_{Tn} are measured and then, they are used to determine in which one of the six 60° – wide sectors of the grid period the voltage is located. Thus, from the signals S_+ and S_- as shown in Fig. 2 *b*, the gate commands for the six IGBT devices $S_{1,2,3,4,5,6}$ are obtained.



a



b

Fig. 2 − Control diagrams: *a* – of the high frequency switches S_+ and S_- for the three single-stage rectifier topologies: the six-switch, the SWISS and the eight-switch rectifiers, *b* – of the low frequency switches S_1, S_2, S_3, S_4, S_5, S_6.

The conventional SWISS unity power factor correction rectifier can be seen in Fig. 3. This rectifier topology has two more IGBT devices (S_+ and S_-) if compared to the six-switch rectifier topology. The former control scheme, which regulates the rectifier output voltage u_{dc} for the six-switch rectifier case is suitable for the SWISS rectifier control case also. Their switching frequency is high (36 kHz) and the gate commands are exactly the signals S_+ and S_-

previously shown in Fig. 2 *a*. The difference is depicted in Fig. 4 and stays in the way of obtaining the gate commands (S_1, S_2, S_3, S_4, S_5, S_6) for the active third harmonic current injection switches which are working at low frequency.

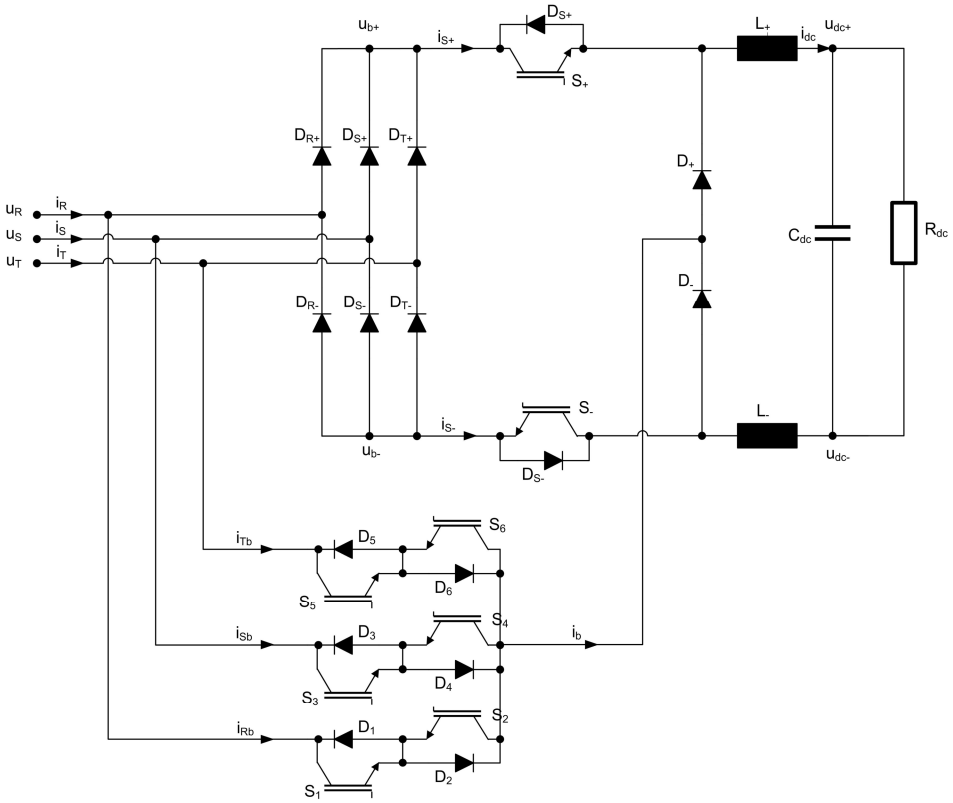


Fig. 3 − SWISS rectifier topology scheme.

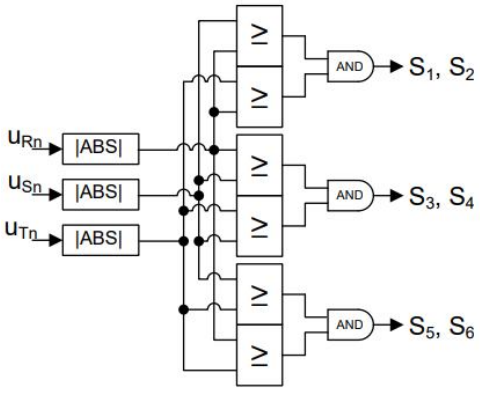


Fig. 4 – Common control of the third harmonic current injection switches for the SWISS and eight-switch rectifiers.

The eight-switch unity PFC rectifier from (Ancuți, 2015) as per Fig. 5 is analyzed in this paper. A particular and different commutation strategy from the one described in (Soreio, 2013) is used in here. The eight-switch and the SWISS unity PFC rectifiers have common implementation control schemes, as previously presented in Fig. 2 *a* and Fig. 4.

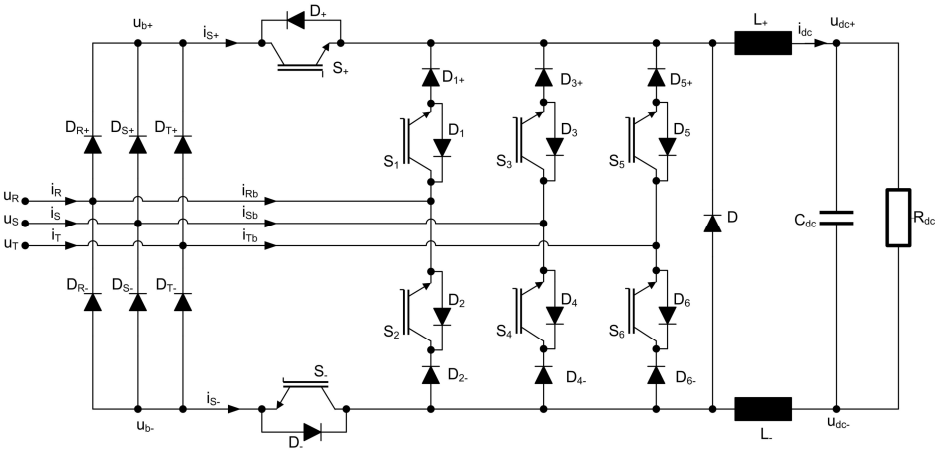


Fig. 5 − Eight-switch rectifier topology scheme.

3. Interleaved High Efficient Unity Power Factor Correction Topologies

The interleaved six-switch unity power factor rectifier is presented in Fig. 6. If compared with the single-stage six-switch rectifier topology presented in the previous chapter, the difference between them consists, first, in the hardware design. The interleaved rectifier has another six more switches added and their corresponding antiparallel diodes.

From the control switching strategy point of view (Fig. 7), it is similar at same point with the one presented in Figs. 2 *a* and 2 *b*, with some amendments. On one hand, the output of the current controller ($\Delta u^{*)}$ is compared with a triangular carrier (PWM 0º) of 18 kHz (which is half of the frequency used for single-stage rectifier topologies as previously presented in chapter 2), resulting the command signals S_{a+} and S_{a-}. On the other hand, the same Δu^{*} is compared with a triangular carrier of 18 kHz, but with 180˚ phase shifted (PWM 180º). Thus, the signals commands S_{b+} and S_{b-} are generated.

These signals are next used for providing the final gate commands for the twelve switches S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8, S_9, S_{10}, S_{11}, S_{12}. For example, the signals S_{a+} and S_{b+} are used to provide the upper stage switches S_{a1} and S_{b1}, respectively the signals S_{a-} and S_{b-} are used to build the lower stage switches S_{a2} and S_{b2}, as shown in Fig. 7 *b*. This is the case of the interleaved six-switch rectifier control strategy.

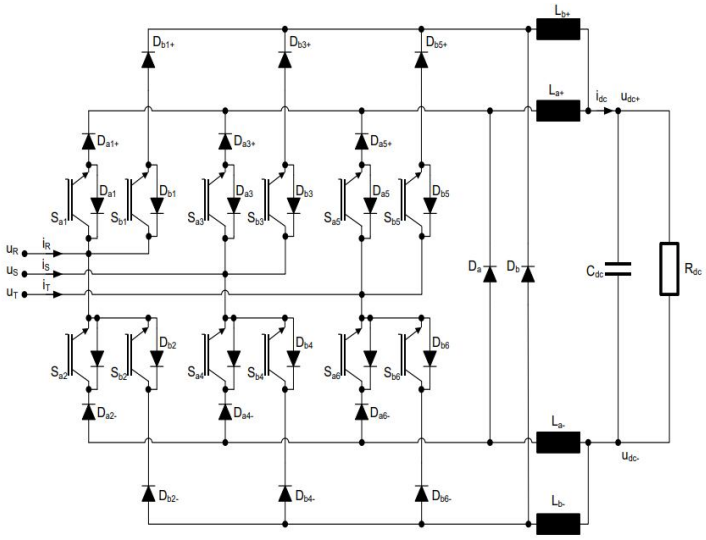
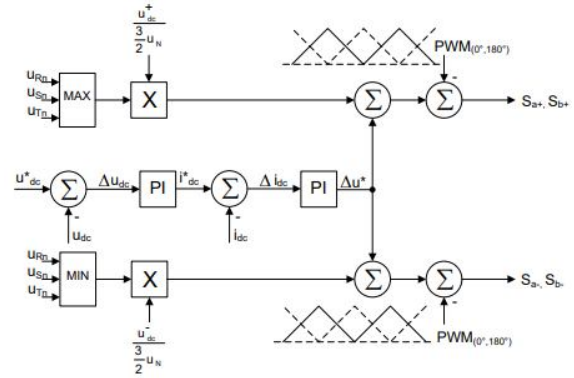
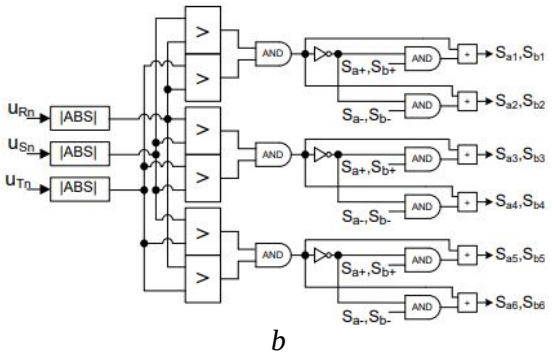


Fig. 6 − Interleaved six-switch rectifier topology scheme.



a



b

Fig. 7 – Control diagrams: *a* – of the three interleaved topologies: interleaved six-switch, interleaved SWISS and interleaved eight-switch rectifiers, *b* – of their twelve switches: S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8, S_9, S_{10}, S_{11}, S_{12}.

The control diagram presented in Fig. 7 *a* is also common for the control strategy of the interleaved SWISS rectifier depicted in Fig. 8. The hardware design of this rectifier has two more IGBTs (S_{b+}, S_{b-}) and two more fast diodes (D_{b+}, D_{b-}) added, if compared with the single-stage Swiss rectifier topology presented previously in Fig. 3.

For the lower part of Fig. 8, meaning the third harmonic injection circuit, the control is as described in the case of single-stage Swiss rectifier topology in chapter 2 (as shown actually in Fig. 4 for the S_1, S_2, S_3, S_4, S_5, S_6 signal generation).

For the interleaved eight-switch configuration topology (Fig. 9), two more IGBTs (S_{b+}, S_{b-}) six more diodes in parallel (D_{1b+}, D_{3b+}, D_{5b+}, D_{2b-}, D_{4b-}, D_{6b-}) and one more fast diode (D_b) are introduced to the single-stage eight-switch topology presented in Fig. 4.

The control strategy for this rectifier topology is the one used also for the former interleaved rectifier, e.g. the interleaved SWISS rectifier, from which the command signals (S_{a+}, S_{a-}, S_{b+}, S_{b-}) are obtained. The same as in the case of interleaved Swiss rectifier, for the interleaved eight-switch rectifier the command signals S_1, S_2, S_3, S_4, S_5, S_6 are also obtained as per Fig. 4.

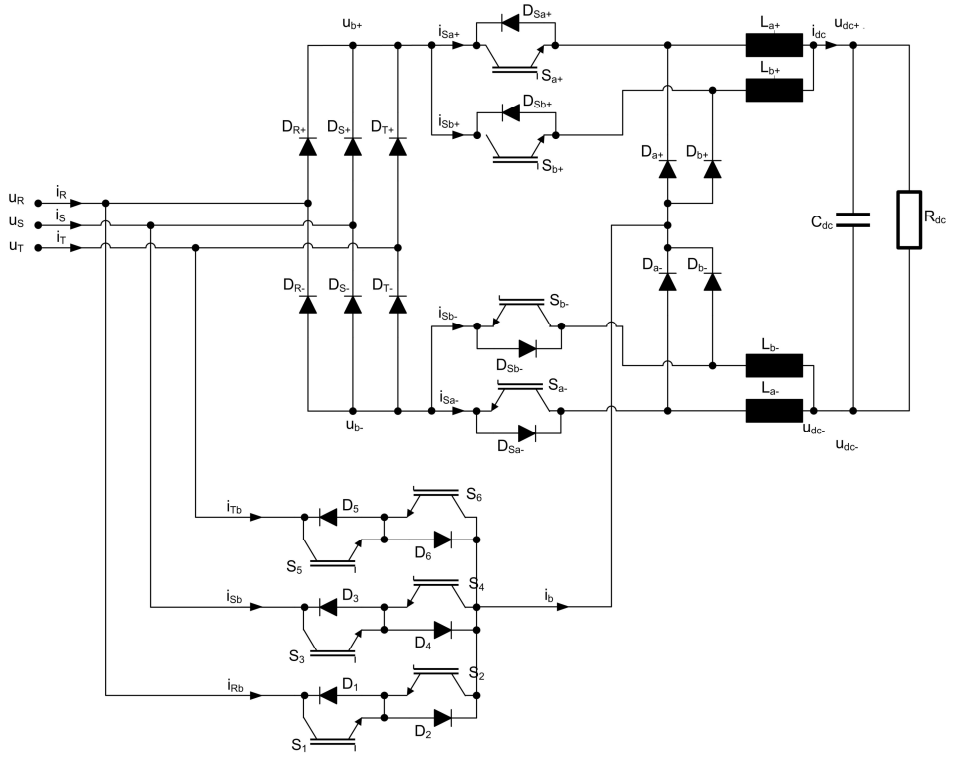


Fig. 8 − Interleaved SWISS rectifier topology scheme.

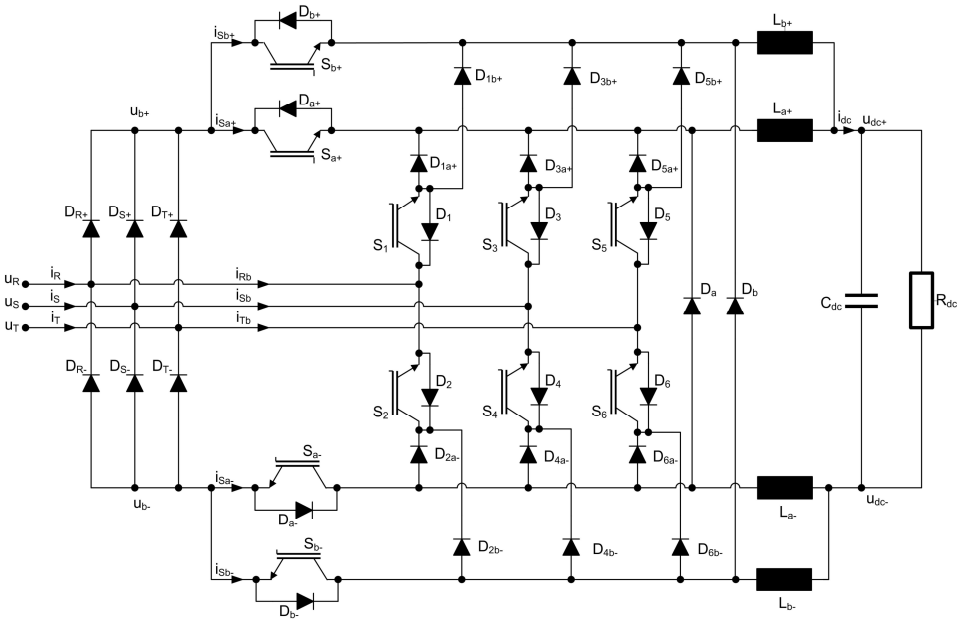


Fig. 9 − Interleaved eight-switch rectifier topology scheme.

4. Simulation Results

The simulation results, for all six unity PFC rectifiers proposed in here, were performed in GECKO Circuits environment and are next presented (see Figs. 10,…,16). One thing should be mentioned from the start, namely that they were obtained for the same operation conditions, as depicted in Table 1 (*e.g.*, for a 7.5 kW output power) and using the catalogue parameters for the power devices as per Table 2.

Table 1
Simulation Model Specifications

Input phase voltages $u_{R,S,T}$ rms value	230 V
Mains frequency f_n	50 Hz
Switching frequency f_{sw}	36 kHz
Interleaved switching frequency f_{sw_int}	18kHz
Rated output power	7.5 kW
Output capacitor C_{dc}	50 µF
DC inductors L_+/L_-	500 µH
Input Filter $L_{R,S,T}$ and $C_{R,S,T}$	85 µH/13.4 µF

Table 2
Components Used in Simulation

Component	Device Description
S_i/D_i	Si T&FS IGBTs, 1,200 V / 25 A, IKW25N120, Infineon
S_{i+}/S_{i-}	Si HighSpeed T&FS IGBTs, IGW40N120H3, Infineon
D_{Ri+}/D_{Ri-}	Si fast recovery diode, DSEP060-12AR, IXYS
D_{i+}/D_{i-}	SiC Schottky diodes, 1,200 V / 20 A, C2D20120A, CREE

As it can be seen, all six unity PFC rectifiers have the input currents (i_R, i_S, i_T) sinusoidal and in phase with the input voltages (u_R, u_S, u_T), thus demonstrating their capability of providing unity power factor correction. Also, it can be noticed that the ripples in the output power P_{out} are smaller for the interleaved rectifier topologies than for the single-stage ones.

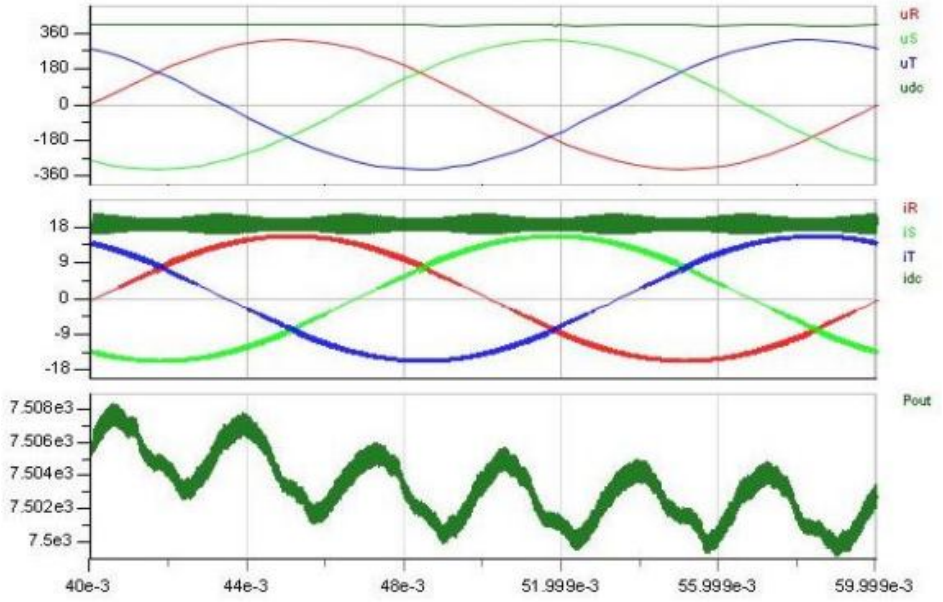


Fig. 10 − Six-switch rectifier: input phase voltages u_R, u_S, u_T, measured dc output voltage u_{dc}, input phase currents i_R, i_S, i_T, measured dc output current i_{dc}, output power P_{out}.

As presented, for the interleaved unity power factor correction rectifier topologies, there are two inductors in parallel for the two DC-link poles. The currents flowing through them are 180º phase-shifted. As consequence, the total input current, has smaller ripple than the one flowing through each individual inductor. Thus, the possibility of reducing the size of the input filter and moving its cutoff frequency higher frequency is inherent.

For each configuration, the losses are computed using special GECKO built-in devices and, then included in the general efficiency equation, as next presented:

$$\eta = P_{\text{out}}/(P_{\text{out}} + P_{c,\text{diodes}} + P_{c,\text{IGBTs}} + P_{sw,\text{IGBTs}}) \quad (1)$$

where: P_{out} represents the output power, $P_{c,\text{diodes}}$ represents the conduction power losses through the diodes, $P_{c,\text{IGBTs}}$ represents the conduction power losses through the IGBT devices and $P_{sw,\text{IGBTs}}$ represents the switching power losses through the IGBT devices.

The simulation results were carried out for rectifiers operation at 7.5 kW. Thus, the efficiency curves once obtained (as shown in Fig. 18), they are compared one to each other and, finally, conclusion are to be drawn: for the interleaved unity power factor correction rectifier topologies, there is a significant gain in efficiency.

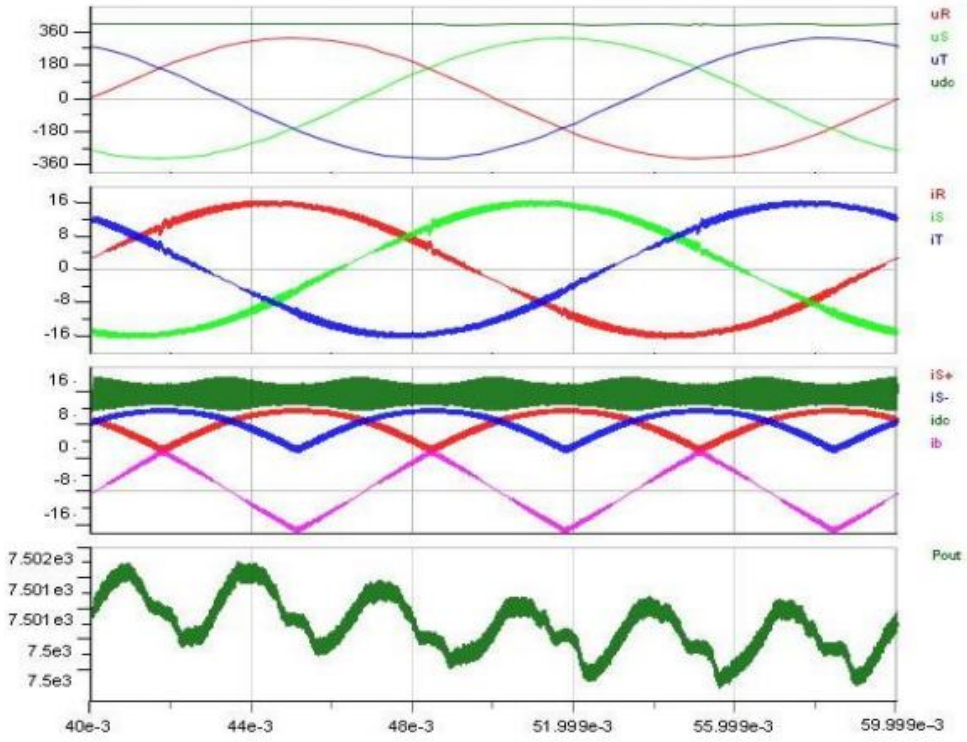


Fig. 11 − SWISS rectifier: input phase voltages u_R, u_S, u_T, measured dc output voltage u_{dc}, input phase currents i_R, i_S, i_T, currents through the high frequency IGBTs on both rectifier stages i_{S+}, i_{S-}, measured dc output current i_{dc}, sum of the phase currents through the current injection switches i_b, measured output power P_{out}.

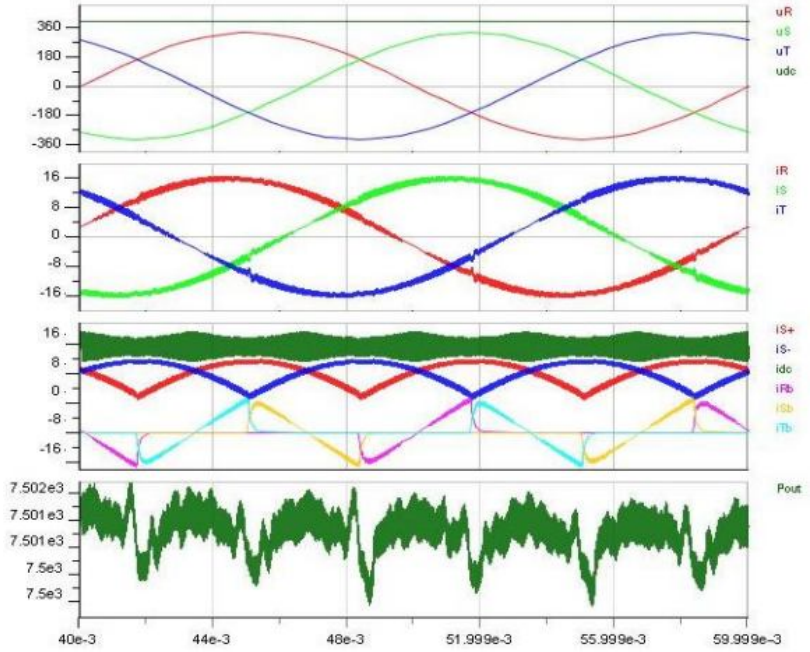


Fig. 12 − Eight-switch rectifier: input phase voltages $u_{R,}$ $u_{S,}$ u_T, measured dc output voltage u_{dc}, input phase currents $i_{R,}$ $i_{S,}$ i_T, currents through the high frequency IGBTs on both rectifier stages i_{S+}, i_{S-}, measured dc output current i_{dc}, phase currents through the current injection switches i_{Rb}, i_{Sb}, i_{Tb}, measured output power P_{out}.

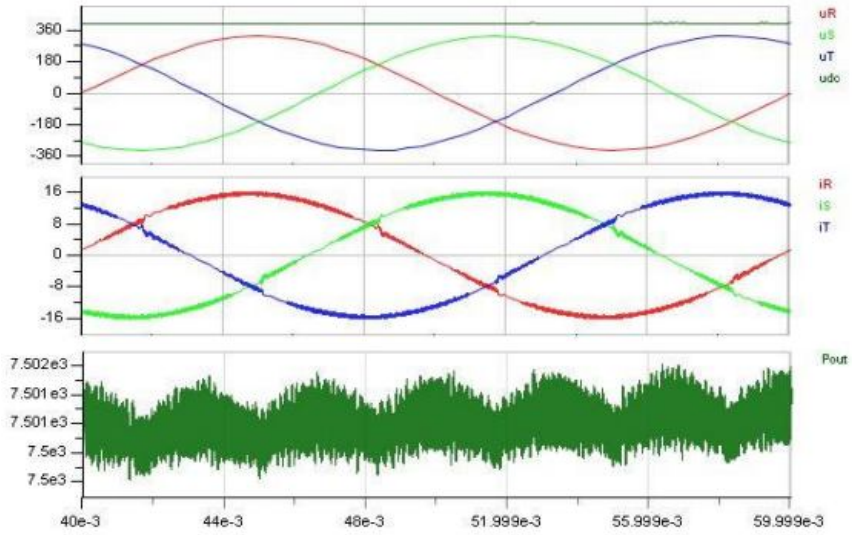


Fig. 13 − Interleaved six-switch rectifier: input phase voltages $u_{R,}$ $u_{S,}$ u_T, measured dc output voltage u_{dc}, input phase currents i_R, i_S, i_T, measured output power P_{out}.

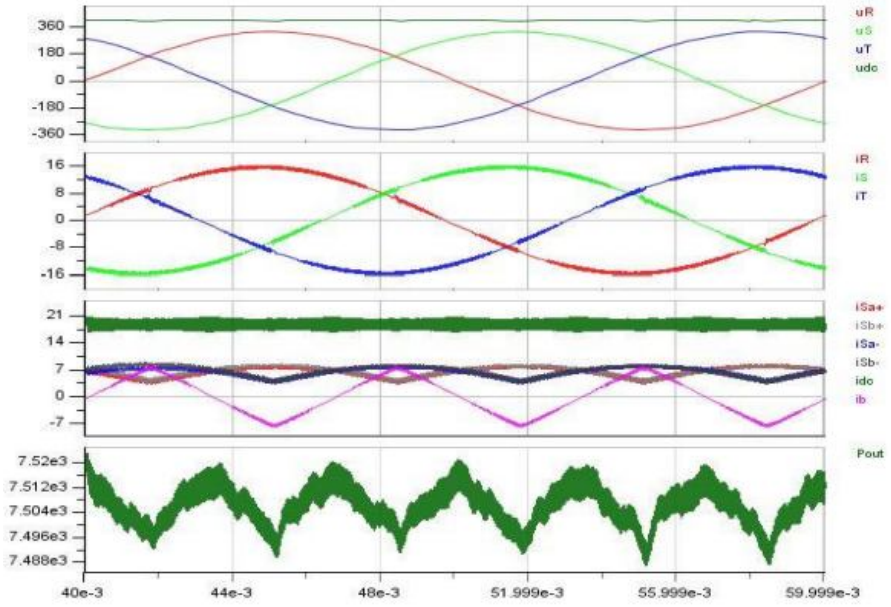


Fig. 14 − Interleaved swiss rectifier: input phase voltages $u_{R,}$ $u_{S,}$ u_T, measured dc output voltage u_{dc}, input phase currents $i_{R,S,T}$, currents through the high frequency IGBTs on both rectifier stages i_{Sa+}, i_{Sb+}, $i_{Sa–}$, $i_{Sb–}$, measured dc output current i_{dc}, sum of the phase currents through the current injection switches i_b, measured output power P_{out}.

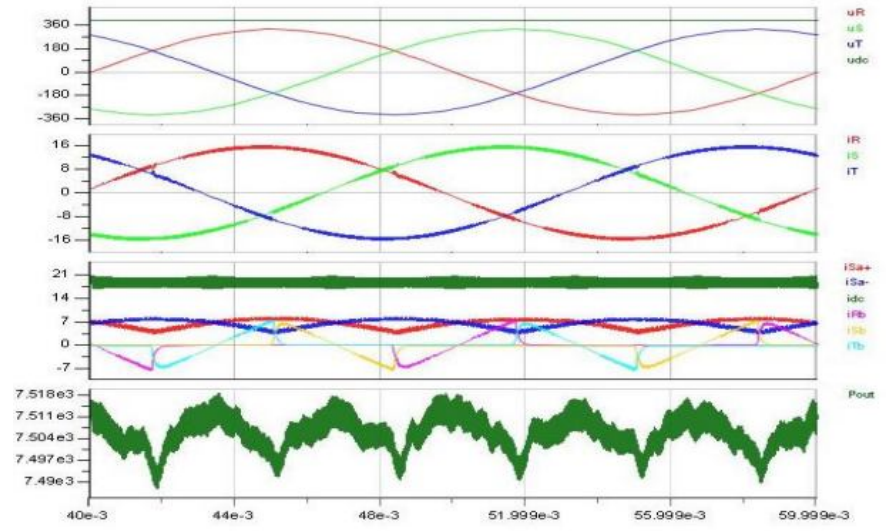


Fig. 15 − Interleaved eight-switch rectifier: input phase voltages u_R, u_S, u_T, measured dc output voltage u_{dc}, input phase currents i_R, i_S, i_T, currents through the high frequency IGBTs on one of the two rectifier stages i_{Sa+}, $i_{Sa–}$, measured dc output current i_{dc}, phase currents through the current injection switches i_{Rb}, i_{Sb}, i_{Tb}, measured output power P_{out}.

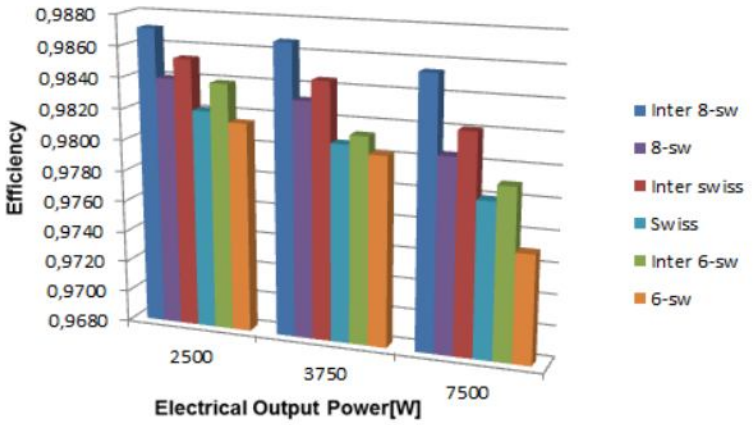


Fig. 16 − Efficiency (η) of all six rectifier topologies (the six-switch, swiss and eight-switch and interleaved topologies) for an output power of 7.5 kW.

5. Conclusion

The three-phase unity PFC rectifier topologies (six) presented in this paper are claiming ultra-high efficiency.

They were implemented in GECKO Circuits simulation environment. Their performances and efficiency evaluation were studied by comparison.

If looking at the results and comparing them, the conclusion was that the interleaved (two-stages) solutions claim higher efficiency levels, while having, in the same time, lower rating values for the switching devices.

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CONVERTOARE CU RANDAMENT RIDICAT CE ASIGURĂ FACTOR DE PUTERE UNITAR

(Rezumat)

Unul dintre subiectele foarte dezbatute şi, care, încă prezintă un larg interes pentru industrie este cel al corecției factorului de putere spre valoarea ideală 1. Acest

lucru se poate realiza cu ajutorul celor şase tipologii de redresoare şi care, aşa cum este prezentat în lucrare se dovedesc a avea randamnet ridicat în jurul valorii de 99%. Cele şase convertoare sunt cunoscute sub denumirea de six-switches, SWISS, eight-switches şi cele trei variante ale lor ce folosesc strategia de comutare intercalată. Această strategie de comutare intercalată implică o tipologie hardware a convertorului pe două nivele şi are marele avantaj de a anula armonicile de intrare pe partea de curent alternativ şi de a reduce fluctuaţiilor tensiunii pe partea current continuu. Astfel, în aceasta lucrare cele şase convertoare de corecţie a factorului de putere sunt evaluate din punct de vedere al eficienţei, pe baza studiilor de simulare efectuate în mediul GECKO Circuits. Şi, în concordanţă cu rezultatele obţinute, se poate concluziona ă este asigurată o eficienţă energetică mai mare pentru soluţiile redresoare reprezentate de cele trei convertoare ce au la bază tipologia pe două nivele, în comparaţie cu cele construite pe un singur nivel.