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A DC-DC BUCK CONVERTER PID TUNING BY MEANS OF POLE-PLACEMENT TECHNIQUE FOR INPUT VOLTAGE DISTURBANCE REJECTION

BY

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Abstract. The present work focuses on tuning the parameters of a digital PID control for a DC-DC Buck converter by means of pole-placement technique. In normal operation, the DC-DC Buck converter may be subject to changes in: reference voltage, input voltage and load current. A good tuning of the control parameters should ensure transient performances within specifications (overshoot and settling time) regardless of these variations. Our proposed PID tuning method is a two steps method. First, a fifth order prototype transfer function that models specific time-domain performances is determined. In the second step, the values of the PID parameters are calculated by imposing the transfer function of the DC-DC Buck converter in closed loop operation to have the same expression as the prototype. In this work, the simulation results obtained for input voltage steps variations are analysed for various imposed time domain specifications, i.e. overshoot and settling time.

Keywords: DC-DC Buck converter; pole-placement; PID tuning.

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1. Introduction

The increased demand of low voltage devices with high performance requirements has resulted in a significant number of researches in the fields of electronics, power and control. It is well known that DC-DC converters are used to efficiently convert electrical power from one voltage level to another one.

While analogue control might provide some advantages, the current trend is to implement the control inside digital circuitry due to the possibility of implementing intelligent control algorithms capable of improving the system performances, (Maksimovic *et al*., 2004).

The most common control scheme used in the industry is the PID due to its simplicity, acceptable performances and robustness. There are various strategies for tuning the coefficients of a PID controller. Some of them are based on analytical tuning rules which are simple to implement and can provide good closed loop behaviour. Based on parameters extracted from the step response, the PID parameters can be computed using classical methods, (Åström & Hägglund, 1995; Skogestard, 2001), such as: Ziegler-Nichols (ZN), Cohen-Coon (CC), Internal Model Control (IMC), Tyreus-Luyben, Aström-Hagglund. Even though these methods provide stable PID controllers, in order to obtain controllers with high performances two methods are commonly used, which can be applied regardless of the control scheme, the pole-zero matching approach and the pole placement method.

The dominant pole placement design approach was introduced in 1992 by Persson and Åström (Persson & Åström, 1992) and since then it was extensively studied (Wang *et al.*, 2008; Dincel & Söylemez, 2014; Mummadi, 2011). In several papers, (Wang *et al.*, 2008; Dincel & Söylemez, 2014), the authors propose a modified Nyquist plot approach to guarantee the dominant pole placement for the case of setpoint tracking. In order to obtain a robust controller for systems with parametric model uncertainties some approaches make use of genetic algorithms (Botto *et al.*, 2002) while others combine pole-placement technique with sensitivity function shaping (Mummadi, 2011).

In addition to the state-of-the-art work, this paper focuses on tuning the parameters of a discrete PID for the case of input signal disturbances. Therefore a pole-placement technique is proposed such as specific time domain performances are achieved for this type of variations. Due to the particular PID control scheme, it is not possible to place the poles of the system at any location. Thus, an analysis of the allowed positions for the poles is conducted.

The paper is organized as follows: Section 2 and Section 3 present the DC-DC Buck Converter application and the linearized model of the system. Section 4 describes the proposed approach for the PID tuning method and in Section 5 the simulation results are presented. The conclusions of the study are drawn in Section 6.

2. DC-DC Buck Converter

As already mentioned, the envisaged application is a DC-DC Buck Converter. This converter transforms a DC input voltage into a stable lower output voltage characterised by a pre-determined value, regardless of the possible fluctuations in input voltage, load current and inherited uncertainties introduced by aging effects, temperature variations or tolerances of the components. The block diagram of the application is presented in Fig. 1.

The converter consists of two parts: an analogue part (power switching devices, output filter and a resistor divider) and a digital feedback path (voltage sensing, compensator and pulse width modulator). The instantaneous output voltage of the converter, V_{OUT}, is scaled by a resistor divider in order to adapt its value to the dynamic range of the analog-to-digital converter. The sensed output voltage is then compared to the reference, V_{REF}, and the error between these two signals is fed to the PID controller. Furthermore, the control is responsible to constantly adjust the duty cycle of the PWM signals that drive the power devices such that the error between the output voltage of the converter and the reference voltage is minimized.

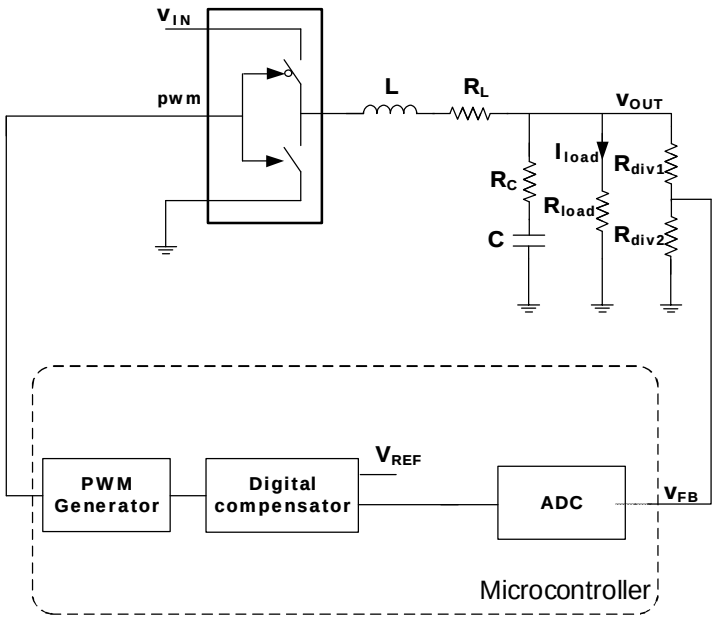


Fig. 1 − Block Diagram of the DC-DC Buck Converter.

For the current case study the following parameters are used for the converter: L = 220 μH, R_L = 1 Ω, C = 16 μF, R_C = 0.21 Ω, f_{SW} = 200 kHz, r_{ds_on} = 0.75 Ω, V_{IN} = 13 V, R_{load} = 470 Ω, V_{REF} = 5 V. The PWM block has a

resolution of 9-bits (K_{PWM} = 719 while the converter output voltage, scaled by the resistor divider (K_{sensor} = 0.148) is sampled by an A/D converter with 12 bits resolution (K_{ADC} = 1240). The considered input voltage test scenarios around the operating point of 13 V, step from 10.5 V to 15.5 V and from 15.5 V to 10.5 V.

3. Linearized Model for DC-DC Buck Converter

Since the pole-placement technique assumes the existence of a transfer function (be it digital or analogue) that describes the behaviour of the application, first we build the linearized model for the DC-DC Buck converter using the approaches presented in (Erickson & Maksimovic, 2004). These methods offer the solution for determining the transfer functions for the open loop behaviour of the converter in analogue domain. However, it can be seen from the block diagram (Fig. 1) that we are dealing with a mixed system that works with both analogue and digital signals. It has been shown in (Amariutei *et al.*, 2015) that for this case study it is better to work only with discrete transfer functions as it offers reliable transient responses similar to the ones obtained through measurements. The obtained discrete linearized model for the application is shown in Fig. 2.

Using the above mentioned approach, three analogue transfer functions of interest were calculated *i.e.*, from input (V_{in}) to output (V_{out}), ($H_{in\_out}(z)$), from reference (pwm) to output ($H_{ctrl\_out}(z)$) and from load current (I_{load}) to output ($Z_{out}(z)$). In order to work with pure discrete signals, the analogue expressions are transformed using the ZOH (Amăriuței *et al.*, 2015).

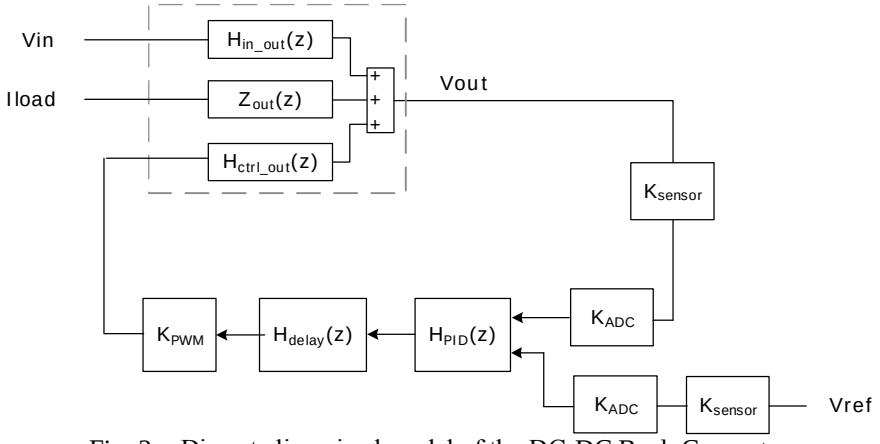


Fig. 2 − Discrete linearized model of the DC-DC Buck Converter

The resulted second order discrete transfer functions have the following generic forms:

– Transfer Function from Input to Output:

$$H_{\text{in\_out}}(z)=\frac{H_{\text{in\_out\_ZOH\_0}}\left(a_1z+a_0\right)}{b_2z^2+b_1z+b_0}; \tag{1}$$

– Transfer Function from Reference Input to Output:

$$H_{\text{ctrl\_out}}(z)=\frac{H_{\text{ctrl\_out\_ZOH\_0}}\left(a_1z+a_0\right)}{b_2z^2+b_1z+b_0}; \tag{2}$$

– Transfer Function from Load Current to Output:

$$Z_{\text{out}}(z)=\frac{Z_{\text{out\_ZOH\_0}}\left(c_2z^2+c_1z+c_0\right)}{b_2z^2+b_1z+b_0}, \tag{3}$$

where the coefficients from the above expressions depend on the values of the components from the analogue part of the converter and the period of the PWM signal.

A classic parallel PID configuration is used for control:

$$H_{\text{PID}}(z)=K_P+K_I\frac{1}{1-z^{-1}}+K_D(1-z^{-1}). \tag{4}$$

The resistor divider, the ADC block and the PWM block are modelled only using their gains with which they contribute to the behaviour of the system. Additionally, a unit delay is added on the feedback path to model the computation time of the microcontroller.

Using this model, the closed-loop behaviour of the DC-DC Buck converter can be described as:

$$V_{\text{out}}(z)=H_{\text{in\_out\_CL}}(z)V_{\text{in}}(z)+H_{\text{ctrl\_out\_CL}}(z)D(z)+Z_{\text{out\_CL}}(z)I_{\text{load}}(z), \tag{5}$$

with the following expressions for the closed loop transfer functions:

– Closed Loop Transfer Function from Input to Output:

$$H_{\text{in\_out\_CL}}(z)=\frac{H_{\text{in\_out}}(z)}{1+T(z)}; \tag{6}$$

– Closed Loop Transfer Function from Reference Input to Output:

$$H_{\text{ctrl\_out\_CL}}(z)=\frac{T(z)}{1+T(z)}; \tag{7}$$

– Closed Loop Transfer Function from Load Current to Output:

$$Z_{\text{out\_CL}}(z)=\frac{Z_{\text{out}}(z)}{1+T(z)}; \tag{8}$$

where T(z) is the loop transfer function expressed by the following equation:

$$\begin{aligned} T(z)&=K_{\text{system}}H_{\text{ctrl\_out}}(z)H_{\text{delay}}(z)H_{\text{PID}}(z),\\ K_{\text{system}}&=K_{\text{sensor}}K_{\text{ADC}}K_{\text{PWM}}. \end{aligned} \tag{9}$$

After several mathematical manipulations, it can be shown that each of the above closed loop transfer functions can be written as a 5th order transfer function with the following expressions:

$$H_{\text{in\_out\_CL}}(z)=\frac{\frac{H_{\text{in\_out\_ZOH\_0}}}{a_1}z^2(z-1)\left(z+\frac{a_0}{a_1}\right)}{z^5+d_4z^4+d_3z^3+d_2z^2+d_1z^1+d_0}, \tag{10}$$

$$\begin{aligned} &H_{\text{ctrl\_out\_CL}}(z)=\\ &=\frac{\frac{K_{\text{system}}H_{\text{ctrl\_out\_ZOH\_0}}}{a_1(K_P+K_I+K_D)}\left(z+\frac{a_0}{a_1}\right)\left(z^2+z\frac{-K_P-2K_D}{K_P+K_I+K_D}+\frac{K_D}{K_P+K_I+K_D}\right)}{z^5+d_4z^4+d_3z^3+d_2z^2+d_1z^1+d_0}, \end{aligned} \tag{11}$$

$$Z_{\text{out\_CL}}(z)=\frac{Z_{\text{out\_ZOH\_0}}(c_2z^2+c_1z+c_0)}{z^5+d_4z^4+d_3z^3+d_2z^2+d_1z^1+d_0}. \tag{12}$$

4. PID Tuning Method

In normal operation, the DC-DC Buck converter may be subject to variations in input voltage, load current or reference voltage. Since the PID control is implemented in software, the reference voltage is set to a pre-defined value of 5 V. Therefore, only disturbance rejection scenarios are of interest. When these fluctuations appear at the input of the converter, the output voltage will exhibit a transient behaviour as in Fig. 3, with time-domain performances dependent on the quality of the control loop.

As mentioned before, the time-domain performances of interest are: the overshoot and the settling time. The overshoot is determined as the maximum value of the output voltage expressed in percentage while the settling time is the time interval from the moment when a perturbation occurs and the moment

when the value of the output voltage remains below 1% of the steady state value.

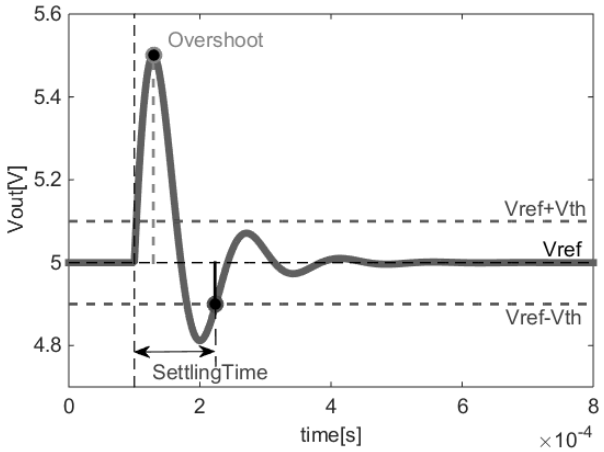


Fig. 3 – Time domain performances of the output voltage for input disturbance step.

In our case we tune the PID to be able to obtain specific values for the time-domain performances, *i.e.* overshoot value smaller than 10% and settling time smaller than 200 us.

The proposed PID tuning method is based on a pole-placement technique performed in the *z*-domain and it consists of two main steps: first a prototype transfer function for the closed loop behaviour of the system is determined and then the values for the PID control such that the DC-DC Buck converter under study has the same transient behaviour as the prototype are calculated.

In the following, each of the above steps is described in more details.

4.1. Determine a Prototype Transfer Function for the Closed Loop Behavior of the System

The fifth order transfer function from (10) can be re-written in the following generic form:

$$H_{\text{in\_out\_CL\_prototype}}(z)=\frac{H_{\text{in\_out\_ZOH\_0}}z^2(z-1)\left(z+\dfrac{a_0}{a_1}\right)}{(z-p_0)\left(z-p_0^*\right)(z-p_1)\left(z-p_1^*\right)(z-p_2)}. \qquad (13)$$

Thus, the transfer function from input voltage to output is characterized by: one pair of dominant complex conjugate poles $\left\{p_0, p_0^*\right\}$, one pair of secondary complex conjugate poles $\left\{p_1, p_1^*\right\}$ and a real pole (p_2). Moreover, it

can be seen that there are a total number of four zeros, from which the one placed on the unit circle has the greatest influence on the dynamics of the output voltage.

It is well-known that extracting an analytical expression for the time-domain performances (overshoot and settling-time) of a 5th order transfer function is almost impossible. Therefore, we first use the pair of dominant poles to build a second order transfer function and then we increase the order by adding three additional poles placed such as the performances are not significantly affected.

Considering a second order analog transfer function of the form (14), the time-domain performances (overshoot and settling time) can be analytically expressed as a function of natural pulsation ω_n and damping ratio ζ.

$$H(s) = k\frac{\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{14}$$

The step response for the above transfer function is given in eq. (15), described by the performances in eqs. (16), (17):

$$y(t) = k\frac{1}{\sqrt{1-\zeta}}\mathrm{e}^{-\zeta\omega_n t}\sin\left(\omega_n\sqrt{1-\zeta^2}t\right), \tag{15}$$

$$Ovsh\,[\%] = k\mathrm{e}^{-\zeta/\sqrt{1-\zeta^2}\tan^{-1}\left(\sqrt{1-\zeta^2}/\zeta\right)}\times 100, \tag{16}$$

$$t_s = -\frac{1}{\zeta\omega_n}\ln\left(\frac{0.01\sqrt{1-\zeta^2}}{k}\right). \tag{17}$$

In order to maintain the same expressions for the performances also in discrete domain, the second order prototype function is ZOH-transformed from (14). The resulted transfer function is given in:

$$H(z) = k\frac{\left[\mathrm{e}^{-\zeta\omega_n T}\sin\left(\omega_n\sqrt{1-\zeta^2}T\right)\Big/\sqrt{1-\zeta}\right](z-1)}{z^2 - 2z\mathrm{e}^{-\zeta\omega_n T}\cos\left(\omega_n\sqrt{1-\zeta^2}T\right) + \mathrm{e}^{-2\zeta\omega_n T}}. \tag{18}$$

Therefore, the position of the dominant poles can be expressed as a function of the angular frequency ω_n and damping ratio ζ as it follows:

$$p_0 / p_0^* = a \pm bj, \tag{19}$$

$$a = \mathrm{e}^{-\zeta\omega_n T}\cos\left(\omega_n\sqrt{1-\zeta^2}T\right), \tag{20}$$

$$b = \mathrm{e}^{-\zeta\omega_n T}\sin\left(\omega_n\sqrt{1-\zeta^2}T\right). \tag{21}$$

So far we have built a second order prototype transfer function but the DC-DC Buck converter requires a 5th order transfer function. Hence, we need to add two secondary complex-conjugate poles and another real pole. All these poles are placed far away from the dominant poles such that the time-domain performances are not affected.

4.2. Calculate the Values of the PID Coefficients so that the DC-DC Buck Converter under Study Has the Same Transient Behavior as the Prototype

The values of the PID control affect only the denominator of the closed-loop transfer function from input to output. Hence, the values of the parameters are determined after solving the equation:

$$Denominator\left(H_{\text{in\_out\_CL}}(z)\right) = Denominator\left(H_{\text{in\_out\_CL\_prototype}}(z)\right), \tag{22}$$

where:

$$\begin{aligned} Denominator\left(H_{\text{in\_out\_CL}}(z)\right) &= z^2(z-1)(b_2z^2+b_1z+b_0)+ \\ &+(a_1z+a_0)\left[z^2\left(K_P+K_I+K_D\right)+z\left(-K_P-2K_D\right)+K_D\right], \end{aligned} \tag{23}$$

and

$$\begin{aligned} Denominator\left(H_{\text{in\_out\_CL\_prototype}}(z)\right) &= (z-p_0)(z-p_0^*)\times \\ &\times(z-p_1)(z-p_1^*)(z-p_2). \end{aligned} \tag{24}$$

As it will be shown, the existence of a real solution for the PID parameters is conditioned by the chosen position of the prototype poles i.e., there will be a region inside the unit circle where the dominant poles cannot be placed.

5. Simulation Results

First, the prototype transfer function of second order is considered to highlight the correspondence between time domain specifications (overshoot and settling time) and position of the dominant poles as shown in Fig. 4.

The results shown in Fig. 4 are normalized as follows: the overshoot is divided to the maximum allowed value 10%, while the obtained settling time

are divided by the maximum allowed value (200 μs). Using these normalizations, we define a performance criterion for a PID set that is calculated as:

$$In-SpecIndex=\max\left(\frac{Ovsh}{Ovsh_{\max}},\ \frac{SettlingTime}{SettlingTime_{\max}}\right). \tag{25}$$

Using this definition for the performance index, the color map from Fig. 4 has the following significance: light gray indicate that both overshoot and settling time are far away from the maximum imposed specifications, while dark gray means that one or both specifications are near the maximum allowed values. The black color of the position for the dominant poles means that one or both specifications are over the maximum allowed value. This color map is used throughout the rest of the paper.

From Fig. 4 it can be seen that only a small region inside the unit circle has to be excluded for the dominant poles in order to be sure that the performance criteria are met. However, this region is further reduced when trying to increase the order of the prototype function from two to five.

In order for the position of the dominant poles to remain valid, at least one real PID set should exist after equalizing the denominator of the 5th order prototype with the denominator of the transfer function for the DC-DC Buck converter. Fig. 5 shows the region of the dominant poles that leads to real PID sets. Thus, the dominant poles should be placed only inside the intersection of valid regions from Figs. 4 and 5.

For illustrating the validity of our solution, in the allowed region, three different locations of the dominant pole are analyzed: one inside the dark grey domain (p_a), one in the middle of light grey (p_b) and one near the inner boundary (p_c). The investigated positions are marked with black in Fig. 6.

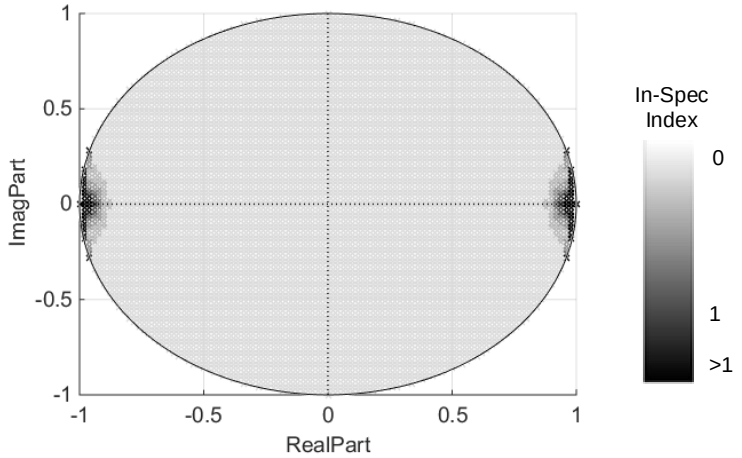


Fig. 4 − Time domain performances for the second order transfer function prototype based on the dominant poles position.

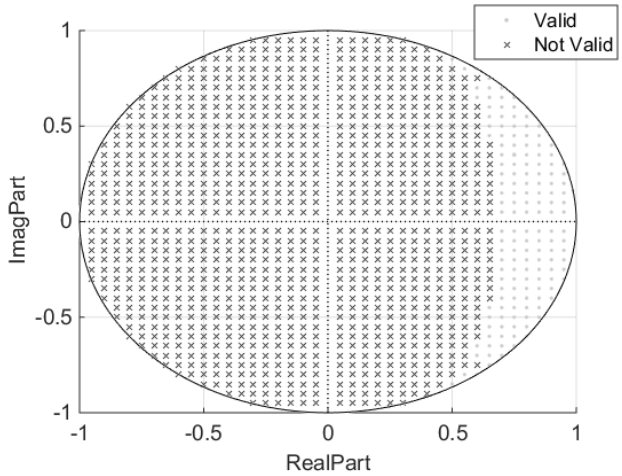


Fig. 5 − Allowed locations for the dominant poles in order to obtain valid parameters for PID control.

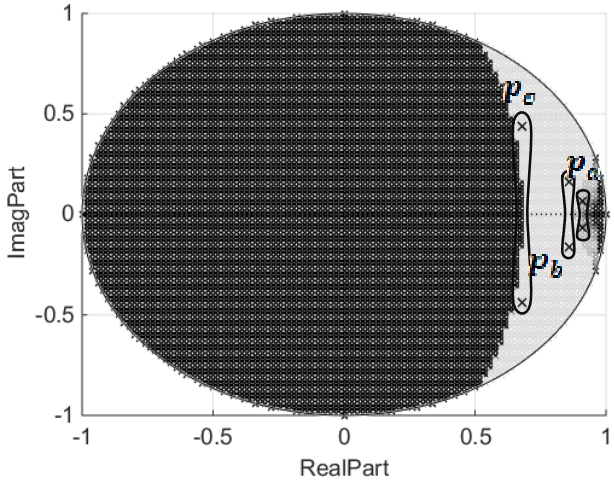


Fig. 6 – Allowed domain for the dominant poles and the locations for the chosen positions of the dominant poles for the further investigation.

For each chosen position of the dominant poles, several locations for the additional poles can be imposed and as a result, several PID sets are obtained. The time-domain performances of the 5th order prototype using all obtained controller configurations are determined. These results are compared with the ones obtained through simulation of the nonlinear model using input steps of 5 V around the operating condition.

In the following the simulation results for each of the three considered locations of the dominant poles are presented.

a) Dominant poles inside the dark gray region (p_a)

Possible locations for the additional poles are shown in Fig. 7 and the corresponding PID values are presented in Fig. 8. The step responses for a positive input step of 5V is shown in Fig. 9 *a*, while the step response for a negative 5V step is presented in Fig. 9 *b*.

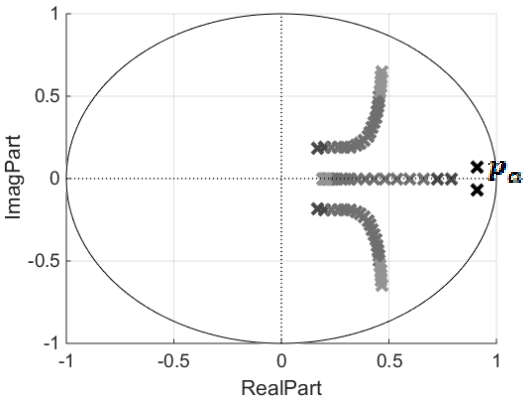


Fig. 7 – Locations of the additional poles.

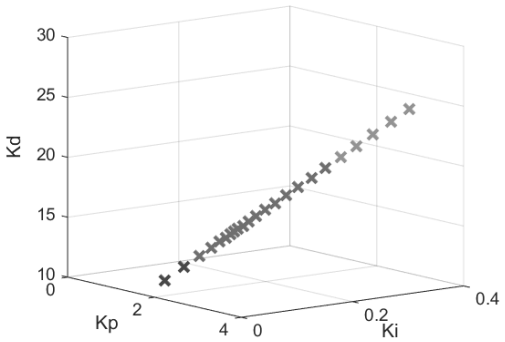


Fig. 8 – PID control parameters.

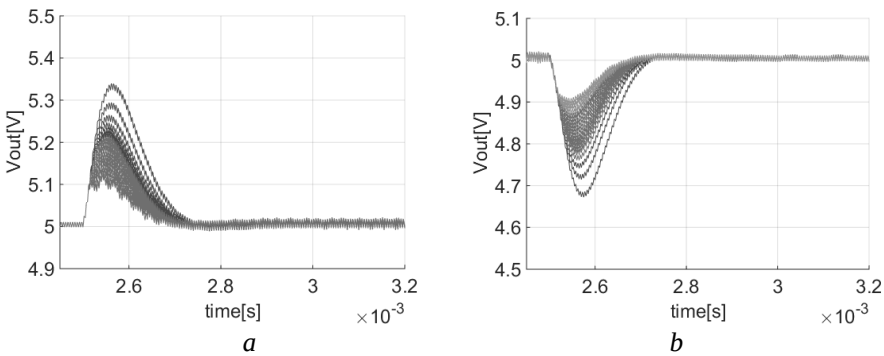


Fig. 9 – Step responses obtained for: a positive input step (*a*), a negative input step (*b*).

It can be seen that the performance index remains in the dark gray region as imposed by the position of the dominant poles.

b) Dominant poles in the middle of light gray region (p_b)

For this case the locations of the secondary poles are shown in Fig. 10. The determined PID values are presented in Fig. 11. And the transient responses are shown in Fig. 12.

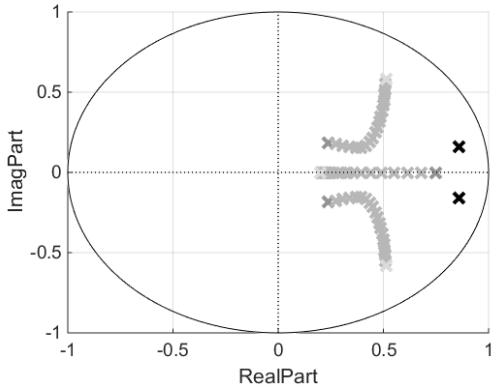


Fig. 10 – Locations of the additional poles.

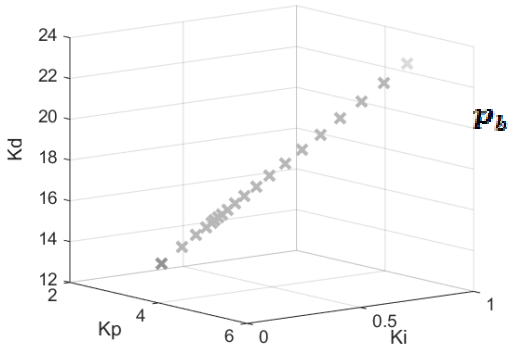
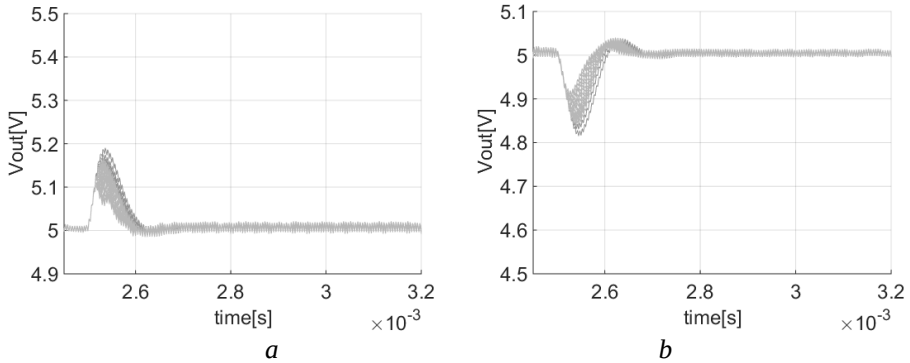


Fig. 11 – PID control parameters.



a *b*

Fig. 12 – Step responses obtained for: a positive input step (*a*), a negative input step (*b*).

As expected the performances are better in this case, therefore this location is preferred.

c) Dominant poles near the inner boundary (p_c)

When the poles are placed near the inner boundary, very few locations for the auxiliary poles are allowed as shown in Fig. 13, and as a consequence only few PID sets are attainable (Fig. 14). The input step responses are presented in Fig. 15.

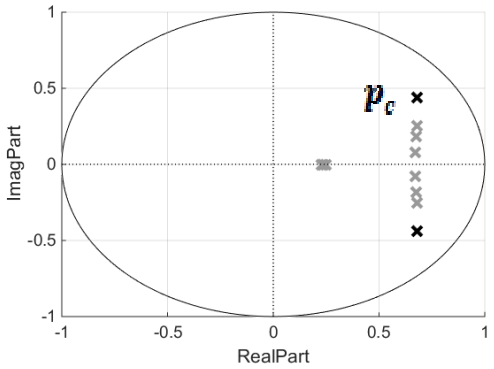


Fig. 13 – Locations of the additional poles.

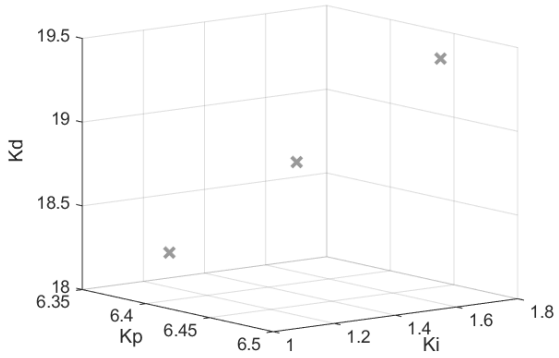
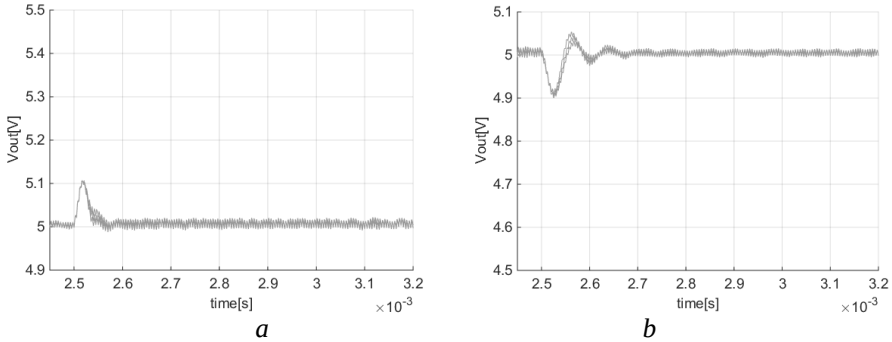


Fig. 14 – PID control parameters.



a *b*

Fig. 15 – Step responses obtained for: a positive input step (*a*), a negative input step (*b*).

In addition to the fact that in this case there are a limited number of choices for the PID values, it can be seen from above figures that the output voltage has also an oscillatory behavior, thus it is not recommended using this location for the dominant poles.

One important observation of this investigation regards placing the dominant poles inside the allowed region (Fig. 6), in order to have an improved rejection of the input voltage perturbations. Using the proposed method, for a set of imposed time domain specifications a position of dominant poles is derived using a second-order prototype transfer function. Moreover, it can be seen that all the PID sets obtained for the previous determined position of dominant poles, have better time domain specifications than the ones obtained using only the second order prototype.

6. Conclusion

This paper presents a method for tuning the parameters of a discrete PID control scheme based on pole-placement technique. Compared to the state of the art, this work focuses on input voltage disturbance rejection. For the DC-DC Buck converter application operating in closed loop, a fifth order prototype transfer function is proposed. The positions of the poles for the imposed prototype are analysed in order to offer specific time domain performances to input voltage steps and to provide solutions for the PID control parameters. Simulation results presented in order to validate the method confirm the effectiveness of the proposed technique.

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METODĂ DE REGLARE A CONTROLULUI DE TIP PID UTILIZÂND TEHNICA DE PLASARE A POLILOR PENTRU REJECȚIA DISTURBAȚIILOR PE TENSIUNEA DE INTRARE LA UN CONVERTOR CC-CC DE TIP BUCK

(Rezumat)

Lucrarea de față se concentrează asupra reglării parametrilor controlului digital de tip PID pentru un convertor CC-CC de tip Buck prin tehnica de plasare a polilor. În funcționarea normală, convertorul CC-CC de tip Buck poate fi supus unor modificări în: tensiunea de referință, tensiunea de intrare şi curentul de sarcină. O reglare bună a parametrilor de control ar trebui să asigure performanțe tranzitorii în limitele specificațiilor impuse (supracreştere şi timp de stabilizare) indiferent de aceste variații. Metoda de reglare a controlului de tip PID propusă constă în doi paşi. Mai întâi, se determină o funcție de transfer prototip de ordin cinci, care modelează performanțele specificate in domeniul timp. În a doua etapă, valorile parametrilor PID se calculează prin impunerea condiției ca funcția de transfer a convertorului CC-CC de tip Buck în funcționarea în buclă închisă să aibă aceeaşi expresie ca şi prototipul. În această lucrare, rezultatele din simulare obținute pentru variații ale tensiunii de intrare de tip treapta sunt analizate pentru diferite specificații impuse în domeniul timp, adică supracrestere şi timp de stabilizare.