BULETINUL INSTITUTULUI POLITEHNIC DIN IAŞI
Publicat de
Universitatea Tehnică „Gheorghe Asachi” din Iaşi
Volumul 64 (68), Numărul 4, 2018
Secția
ELECTROTEHNICĂ. ENERGETICĂ. ELECTRONICĂ

A NEW SYSTOLIC ARRAY ALGORITHM BASED ON BAND-CORRELATION STRUCTURE AND AN EFFICIENT VLSI ARCHITECTURE FOR THE ODD-TIME GDHT

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Received: October 19, 2018
Accepted for publication: November 29, 2018

Abstract. Using two input restructuring sequences a new VLSI algorithm for 1-D odd-time generalized Hartley transform (GDHT) for an efficient VLSI architecture based on systolic array architectural paradigm. The proposed VLSI architecture has appealing topological features and high performances. The new algorithm is based on a modular and regular computational structure called band-correlation. Using the proposed algorithm we can obtain an efficient VLSI architecture for odd-time GDHT having a high speed at a low hardware complexity.

Keywords: generalized discrete Hartley transform; discrete transforms; systolic arrays; systolic algorithms; VLSI algorithms.

1. Introduction

The generalized discrete Hartley transform (GDHT) (Hu *et al.*,1992) has been proved to efficiently replace the generalized discrete Fourier transform

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(GDFT) when the input sequence is real. It has the same useful applications as GDFT in many fields as designing filter banks, signal representation, computing convolutions and fast computation of DFT. One of the most useful forms of

GDHT is the odd-timed GDHT. There are many software solutions for GDHT but until now a few efficient hardware algorithms has been proposed for DHT (Chiper, 2005; Pan,1997; Chiper,2013) and especially for GDHT (Chiper, 2012; Chiper *et al*.,2004). Due to the fact that GDHT has a high computational complexity, in many real-time applications it is necessary to find efficient dedicated VLSI-based hardware structures to satisfy the requirements of the specific applications.

In real-time applications it is necessary to design VLSI hardware accelerators that can speed up the execution of the GDHT transform. In order to do this is necessary to design new VLSI algorithms or to reformulate existing algorithms for odd-time GDHT in a such manner that an efficient VLSI implementation can be obtained.

It is well known that the efficiency of a hardware algorithm is due not only to the computational one but especially to the communication complexity. This is due to the fact that data movement plays a key role in a VLSI implementation. So, the FFT algorithm that has a very good computational complexity is not so good from a VLSI implementation point of view.

Cycle convolution and circular correlation algorithms have remarkable advantages over other ones due to its efficient input/output and data transfer operations. These computational structures can be efficiently implemented in VLSI using distributed arithmetic (White, 1989) or systolic arrays (Kung,1982). Thus, several solutions have been proposed for a VLSI implementation of some DSP algorithms based on cyclic convolution or circular correlation (Meher, 2006; Chiper, 2007; Cheng, 2006; Chiper *et al*., 2011).

The important advantages of the circular correlation or cycle convolution from a VLSI implementation point of view can be extended to other structures as for example skew-circular and pseudo-circular correlations or band-correlation (Chiper, 2011a,b; Chiper, 2017).

In this paper we propose a new systolic array algorithm for odd-time GDHT using two band-correlation structures. These structures have a regular and modular form and can be computed in parallel resulting thus a high throughput VLSI implementation. In order to obtain an efficient VLSI algorithm we have used an appropriate restructuring method of the 1-D odd-time GDHT into such regular structures. All the advantages of a circular correlation based implementation as regularity, modularity, low I/O cost and a reduced data management scheme can be obtained with the proposed computational structures.

The rest of the paper is organized as follows: in Section **2** an efficient formulation of 1-D odd-time GDHT is presented using an example for a 1-D GDHT of length $N = 13$ that can be used to obtain a unified VLSI implementation. In Section **3** we discuss some considerations about a VLSI

implementation of the proposed algorithm using the systolic array architectural paradigm. Conclusions are presented in Section **4**.

2. **Systolic Algorithm for the Odd-Time GDHT**

To illustrate our decomposition method, we use an example with the transform length $N = 13$ and the primitive root $g = 2$.

The odd-time generalized DHT of the input sequence $\{x(i): i = 0, 1,\ldots, N-1\}$ is defined as:

$$Y(k) = \sum_{i=0}^{N-1} x(i)\, cas\left[(2i+1)k\alpha\right], \tag{1}$$

where: $\alpha = \pi / N$, and $cas(\theta) = \cos(\theta) + \sin(\theta)$.

If the transform length N is a prime number, its computation can be reformulated for an efficient VLSI implementation as follows:

$$\begin{bmatrix} Y(1) \\ Y(2) \\ Y(3) \\ Y(4) \\ Y(5) \\ Y(6) \end{bmatrix} = \begin{bmatrix} H_C(1)\cdot\cos(\alpha) \\ H_C(2)\cdot\cos(2\alpha) \\ H_C(3)\cdot\cos(3\alpha) \\ H_C(4)\cdot\cos(4\alpha) \\ H_C(5)\cdot\cos(5\alpha) \\ H_C(6)\cdot\cos(6\alpha) \end{bmatrix} + \begin{bmatrix} H_S(1)\cdot\sin(\alpha) \\ H_S(2)\cdot\sin(2\alpha) \\ H_S(3)\cdot\sin(3\alpha) \\ H_S(4)\cdot\sin(4\alpha) \\ H_S(5)\cdot\sin(5\alpha) \\ H_S(6)\cdot\sin(6\alpha) \end{bmatrix}, \tag{2}$$

$$\begin{bmatrix} Y(12) \\ Y(11) \\ Y(10) \\ Y(9) \\ Y(8) \\ Y(7) \end{bmatrix} = -\begin{bmatrix} H_C(1)\cdot\cos(\alpha) \\ H_C(2)\cdot\cos(2\alpha) \\ H_C(3)\cdot\cos(3\alpha) \\ H_C(4)\cdot\cos(4\alpha) \\ H_C(5)\cdot\cos(5\alpha) \\ H_C(6)\cdot\cos(6\alpha) \end{bmatrix} + \begin{bmatrix} H_S(1)\cdot\sin(\alpha) \\ H_S(2)\cdot\sin(2\alpha) \\ H_S(3)\cdot\sin(3\alpha) \\ H_S(4)\cdot\sin(4\alpha) \\ H_S(5)\cdot\sin(5\alpha) \\ H_S(6)\cdot\sin(6\alpha) \end{bmatrix}, \tag{3}$$

where we have introduced two auxiliary output sequences $\{H_c(i): i = 0, 1,\ldots, (N-1)/2\}$ and $\{H_S(i): i = 0, 1,\ldots, (N-1)/2\}$ that are computed as:

$$\begin{bmatrix} H_C(1) \\ H_C(2) \\ H_C(3) \\ H_C(4) \\ H_C(5) \\ H_C(6) \end{bmatrix} = \begin{bmatrix} x_C(0) + 2\cdot T_C(1) \\ x_C(0) + 2\cdot T_C(2) \\ x_C(0) + 2\cdot T_C(3) \\ x_C(0) + 2\cdot T_C(4) \\ x_C(0) + 2\cdot T_C(5) \\ x_C(0) + 2\cdot T_C(6) \end{bmatrix}, \tag{4}$$

$$\begin{bmatrix} H_S(1) \\ H_S(2) \\ H_S(3) \\ H_S(4) \\ H_S(5) \\ H_S(6) \end{bmatrix} = \begin{bmatrix} x_C(0) + 2 \cdot T_S(1) \\ x_C(0) + 2 \cdot T_S(2) \\ x_C(0) + 2 \cdot T_S(3) \\ x_C(0) + 2 \cdot T_S(4) \\ x_C(0) + 2 \cdot T_S(5) \\ x_C(0) + 2 \cdot T_S(6) \end{bmatrix}. \tag{5}$$

Where we have introduced two other auxiliary output sequences $\{T_c(i): i = 0,1,...,(N-1)/2\}$ and $\{T_S(i): i = 0,1,...,(N-1)/2\}$ that can be computed using a special computational structure called band-correlation that can be efficiently implemented using systolic arrays as will be seen further on.

The two auxiliary output sequences are computed using eqs. (6) and (7) as follows:

$$\begin{bmatrix} T_C(2) \\ T_C(4) \\ T_C(5) \\ T_C(3) \\ T_C(6) \\ T_C(1) \end{bmatrix} = \begin{bmatrix} \cos(4a) & \cos(8a) & \cos(3a) & \cos(6a) & \cos(12a) & \cos(11a) \\ \cos(8a) & \cos(3a) & \cos(6a) & \cos(12a) & \cos(11a) & \cos(9a) \\ \cos(3a) & \cos(6a) & \cos(12a) & \cos(11a) & \cos(9a) & \cos(5a) \\ \cos(6a) & \cos(12a) & \cos(11a) & \cos(9a) & \cos(5a) & \cos(10a) \\ \cos(12a) & \cos(11a) & \cos(9a) & \cos(5a) & \cos(10a) & \cos(7a) \\ \cos(11a) & \cos(9a) & \cos(5a) & \cos(10a) & \cos(7a) & \cos(a) \end{bmatrix} \times \begin{bmatrix} x_C(2) + x_C(11) \\ x_C(4) + x_C(9) \\ x_C(5) + x_C(8) \\ x_C(3) + x_C(10) \\ x_C(6) + x_C(7) \\ x_C(1) + x_C(12) \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} T_S(2) \\ T_S(4) \\ T_S(5) \\ T_S(3) \\ T_S(6) \\ T_S(1) \end{bmatrix} = \begin{bmatrix} \cos(4a) & \cos(8a) & \cos(3a) & \cos(6a) & \cos(12a) & \cos(11a) \\ \cos(8a) & \cos(3a) & \cos(6a) & \cos(12a) & \cos(11a) & \cos(9a) \\ \cos(3a) & \cos(6a) & \cos(12a) & \cos(11a) & \cos(9a) & \cos(5a) \\ \cos(6a) & \cos(12a) & \cos(11a) & \cos(9a) & \cos(5a) & \cos(10a) \\ \cos(12a) & \cos(11a) & \cos(9a) & \cos(5a) & \cos(10a) & \cos(7a) \\ \cos(11a) & \cos(9a) & \cos(5a) & \cos(10a) & \cos(7a) & \cos(a) \end{bmatrix} \times \begin{bmatrix} x_S(2) + x_S(11) \\ x_S(4) + x_S(9) \\ x_S(5) + x_S(8) \\ x_S(3) + x_S(10) \\ x_S(6) + x_S(7) \\ x_S(1) + x_S(12) \end{bmatrix} \tag{7}$$

where: $a = 2\alpha$.

We have used two auxiliary input sequences, defined as:

$$\begin{aligned} &x_C(N-1) = x(N-1) \\ &x_C(i) = x(i) - x_C(i+1) \end{aligned} \quad \text{for } i = N-2,...,0 \tag{8}$$

$$\begin{aligned} &x_S(N-1) = x(N-1) \\ &x_S(i) = x(i) + x_S(i+1) \end{aligned} \quad \text{for } i = N-2,...,0 \tag{9}$$

and appropriate permutation of the Galois Field of the indexes:

$$\psi(k) = \begin{cases} \varphi(k) & \text{if} \quad \varphi(k) \le (N-1)/2 \\ \varphi(k + (N-1)/2) & \text{otherwise} \end{cases} \tag{10}$$

$$\varphi(k) = < g^K >_N \tag{11}$$

3. A VLSI Implementation Discussion

Using the algorithm presented in Section **2** we can obtain an efficient VLSI systolic array using a dependence-graph based synthesis procedure (Kung, 1988). Using this design procedure we can implement eqs. (6) and (7) using two linear systolic arrays working in parallel as shown in Fig. 1.

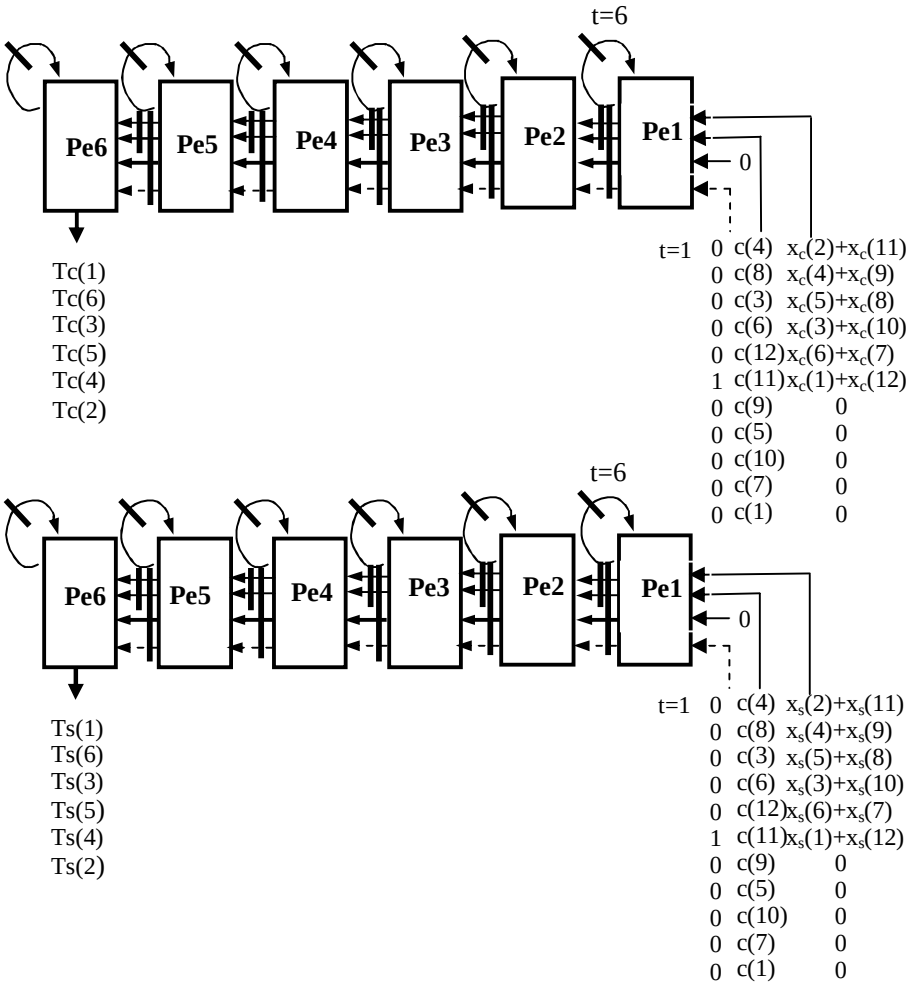

Fig. 1 – The systolic arrays that implement the hardware core of the proposed VLSI architecture.

These systolic arrays represent the hardware core of the architecture used for the VLSI implementation of the derived algorithm. We can obtain a further reduction of the hardware complexity using an appropriate hardware sharing method as that proposed in (Chiper, 2005b) to unify the two systolic

arrays presented in Fig. 1. The function of the processing elements Pe from Fig. 1 is presented in Fig. 2.

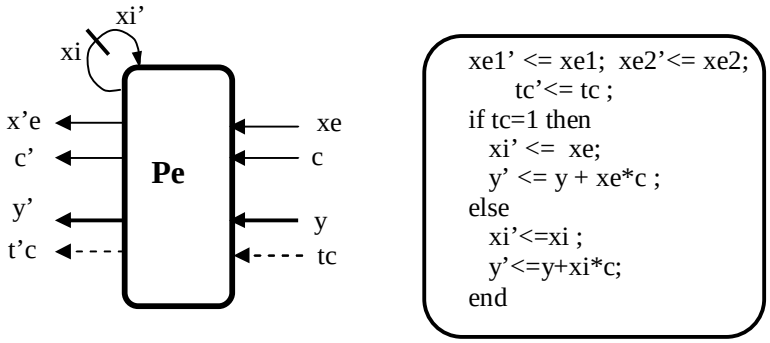

Fig. 2 – The function of the processing elements Pe from Fig. 1.

It can be seen from Fig. 2 that each processing element consists of a multiplier, an adder and a multiplexer that is used to properly select the input data in each multiplier.

Using the so-called tag control bits (Jen *et al.*,1988) we can control the input data to be correctly stored in each processing elements in a such manner that all the input channels to be placed at one of the two ends of the linear systolic array.

It can be seen from Fig. 1 that the input data $x(i) + x(N - i)$ and $c(i)$ are flowing through the systolic array at a half rate of the partial results in such a manner that each input data will meat the right data at the right moment in the right processor. This is a very important condition in order to obtain the correct results at the end of the linear systolic arrays.

This architecture offers a high processing speed by using pipelining and parallelism. The high rate of the processing inside of the array will involve a high volume of input data to be sent to the systolic array. It is the so called I/O bottle neck that will limit the speed performances of a such architecture.

In our solution the so-called I/O bottleneck is avoided by using each data in as many processing elements as possible.

4. Conclusions

In this paper is proposed a new VLSI algorithm for 1-D odd-time GDHT that can be used to obtain an efficient VLSI architecture based on systolic array architectural paradigm. The proposed VLSI algorithm is based on a regular and modular computation structure called band-correlation. It was shown that this computational structure can be implemented in VLSI using the systolic array architectural paradigm with the same appealing features for a VLSI implementation and high speed performances as cyclic convolution and circular correlation. The two band-correlations can be computed in parallel thus

resulting a high throughput VLSI implementation. The architecture that can be obtained has high performances and good topological properties well suited for a VLSI implementation.

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UN NOU ALGORITM SISTOLIC BAZAT PE STRUCTURA BAND-CORRELATION ŞI O ARHITECTURĂ VLSI EFICIENTĂ PENTRU TRANSFORMATA HARTLEY DISCRETĂ GENERALIZATĂ DE TIP ODD-TIME

(Rezumat)

În această lucrare a fost propus un nou algoritm VLSI pentru transformata discrete Hartley generalizată de tip odd-time care poate fi folosit pentru a obține o arhitectură VLSI eficientă bazată pe paradigm arhitecturală sistolică.

Algoritmul VLSI propus se bazează pe o structură computațional regulate şi modular denumită band-correlation. S-a arătat că această structură computațională poate fi implementată efficient în VLSI ustilizând paradigm arhitecturală denumită arie sistolică cu aceleaşi caracteristici atrăgătoare din punct al implementării VLSI şi a performanțelor înalte de viteză ca şi convoluția ciclică sau corelația circular. Cele două band-correlations pot fi procesate în parallel rezultând astfel o implementare VLSI cu un throughput ridicat. Arhitectura VLSI ce poate fi astfel obținută are performanțe înalte şi proprietăți topologice foarte bune, adecvate implementării VLSI.