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ON THE RELIABILITY PERFORMANCE DEGRADATION DUE TO MISALIGNMENT OF ZERO-VOLTAGE TRANSITION RESONANT CONVERTER OPERATION

BY

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Abstract. The resonant converters are used in a wide range of applications due to their advantage in reducing converter switching power loss. However, their control requires a continuous matching of the switching moment to the input source, load current or parameter variation. If the resonant converter is switched before or after the resonant swing ends, more loss is actually added to the system, operating temperature rises and the reliability of the converter is negatively affected. This article is analyzing this problem for the particular case of Zero-Voltage Transition (ZVT) and estimates the effects of a wrong timing in the control of a resonant converter onto the converter reliability.

Keywords: buck converter; resonant converter; reliability; thermal stress; computer analysis.

1. Introduction

The technological evolution of power electronics reached a saturation of performance attributes and the efforts are now directed towards newer performance criteria. For this reason, a considerable amount of research has been dedicated to reliability, lifetime, or failure rate calculation for various

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power converter solutions (Blaabjerg, 2012; Butnicu & Neacşu, 2019). The industry responded with a set of dedicated standards (Anon, 1990; Anon, 2011*)*. This article falls within the same category of works dedicated to analysis of reliability implications of modern converter solutions. A simple resonant buck converter is considered as a case study, and conclusions drawn herein can easily be expanded to other resonant converter classes. Resonant converters have been introduced in research and industry to reduce the switching loss of power semiconductor devices. The switching loss is usually calculated as a product between instantaneous voltage and current, during a transient. All through a switching process of a power semiconductor device, this product is far from zero due to delays and finite transition times. Special resonant circuits are designed and added near power semiconductor switches in order to make the voltage or current stay at or near zero during the switching process. A reduction of switching loss results and the power semiconductor device is therefore operated at lower temperature. In some cases, the saved power is larger than the inherent loss in added components and control, and an overall efficiency improvement occurs. Obviously, there is a tradeoff between the supplementary cost with the addition of resonant circuit and advanced control method, *versus* the reduction in temperature and potential system efficiency improvement. While the difficulties with the proper control timing for such a resonant converter are known, there is very little documentation on the adverse effects of using this technology. This article tries to fill this gap and to discuss reliability-related effects of an improper control. A multitude of things can alter a proper timing diagram. The less obvious ones relate to the resonant components themselves. Recent studies (Overton *et al*., 1993; Kindmark & Rosen, 2013) dedicate ample efforts to ageing and after-shock variation of capacitance and inductance of various technologies for passive components. Without considering any or all, this article studies the total effects of control mis-alignment due to parameter variation.

Resonant buck converters are used in many applications, under different voltage and current demands. The failure rate for each class of applications has a different structure. For instance, low-voltage high-current converters used in telecom and computer applications have the system failure rate strongly depending on the output capacitor bank. Conversely, solar applications, with converters operated at higher voltage and lower current, have a failure rate strongly dependent on the power semiconductor devices due to their limited capacity of the storage bank. This article limits the study to the implications of parameter variation to the failure rate of the power semiconductor module only, considering that the other filter passive components would behave analogously with or without a resonant circuit, within a given application. While solutions for either of Zero-Current Transition (ZCT) and Zero-Voltage Transition (ZVT) are reported, this paper focuses on the ZVT converters, which is the solution more common in practice. The ZVT converter is usually controlling the output voltage with a variable switching frequency. Contemporary integrated circuits

limit the frequency variation range with external R, C components. Similarly, the digital implementation also tends to keep the variation limited. Some research efforts tend to inject additional signals in the reference waveform to reduce the apparent switching frequency range (Kolar, 2014, 2016).

After the problem description in Section **1**, Section **2** reviews the theory behind the resonant buck converter, Section **3** comments on the ageing and after-shock variation of parameters, Section **4** illustrates practically the operation with mis-alignment control, Section **5** comments on different methods used for reliability calculation, and Section **6** sums up conclusions.

The main contributions of the article are as follows:

(1) Brings into discussion – for the first time – the problem of misalignment control of resonant converters and quantifies analytically its effects on reliability.

(2) Reviews literature and sums up the possible causes for ageing and after-shock parameter variations.

(3) Illustrates practically, by simulation and experiment, the thermal effects of control misalignment.

(4) Defines a figure of merit for the reliability deterioration with control mis-alignment, for a sample application.

2. Resonant Buck Converter

The resonant buck converter circuit starts from a conventional buck converter where a series inductance ***Lr*** and a parallel capacitor ***Cr*** have been added near the main power switch. Fig. 1 illustrates this technical solution.

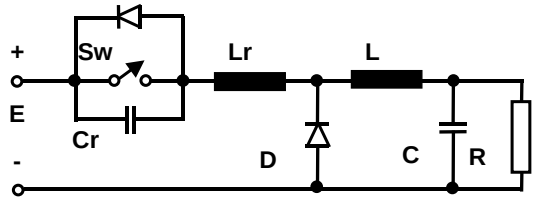

Fig. 1 – Principle of the Resonant Buck Converter.

This section presents a quick analysis of the ideal resonant processes. Our analysis starts with the switch in conduction, and the parallel resonant capacitor ***Cr*** discharged. A zero-voltage is clamped to the capacitor during the conduction interval. The constant load current flows through the resonant inductor ***Lr.*** As soon as the switch is turned off, the current flows through capacitor, and its voltage increases linearly:

$$v_{C_r}(t) = \frac{I_L}{C_r} \cdot t. \tag{1}$$

By difference and considering zero voltage drop across the resonant inductor at constant current, the buck diode sees a voltage (cathode-to-anode):

$$v_D(t) = E - \frac{I_L}{C_r} \cdot t. \tag{2}$$

As soon as the diode ***D*** has a positive bias, it turns-on and re-routes the load current. The conduction time interval before the diode turns-on can be calculated with

$$t_1 = \frac{E}{I_L} \cdot C_r. \tag{3}$$

The components (L_r and C_r) added to the circuit for the resonant swing, can be characterized jointly with a resonant frequency f_r and a characteristic impedance Z_r

$$f_r = \frac{1}{T_r} = \frac{1}{2\pi\sqrt{L_r C_r}}, \tag{4}$$

$$Z_r = \sqrt{\frac{L_r}{C_r}}. \tag{5}$$

This way, the previous time interval t_1 can be calculated in dependence with the new variables

$$t_1 = \frac{E}{I_L} \cdot C_r = \frac{E}{I_L} \cdot \frac{1}{\omega_r Z_r}. \tag{6}$$

Equation (6) becomes a strong design criterion. The time interval t_1 has to be considered much smaller than the switching period of the buck converter so that the average of the voltage pulses and the harmonic content are not affected. Both components, L_r and C_r, have to be selected to match this design rule. Next, the load current passes through the buck diode and the switch remains in the OFF state. The input voltage E equals the sum of voltage drops across L_r and C_r. Before this moment, the inductor had zero voltage drop.

$$L_r C_r \frac{\mathrm{d}v_{C_r}(t)}{\mathrm{d}t^2} + v_{C_r}(t) = E. \tag{7}$$

The voltage across the resonant capacitor C_r increases from E to a peak value, then decreases to zero, after a sinusoidal law:

$$v_{C_r}(t) = E + Z_r I_L \sin\left[\omega_r \left(t - t_1\right)\right]. \tag{8}$$

The peak of the capacitor voltage can also be considered as the maximum voltage drop across the power switch, and it equals:

$$v_{C_r}(\max) = E + Z_r I_L. \tag{9}$$

The moment of time when capacitor voltage reaches zero results as:

$$t_2 = t_1 + \frac{1}{\omega_r}\left[\pi + \arcsin\left(\frac{E}{Z_r I_L}\right)\right]. \tag{10}$$

This time interval is the minimum duration of the off-state for the main switch. The current through L_r and C_r results as:

$$i_{C_r}(t_2) = i_{Lr}(t_2) = -I_L\sqrt{\left[1-\left[\frac{E}{Z_r I_L}\right]^2\right]}. \tag{11}$$

Since the resonant current adds up to the load current, through the output diode, the current through the output diode at t_2 will be:

$$i_D(t_2) = I_L + I_L\sqrt{\left[1-\left[\frac{E}{Z_r I_L}\right]^2\right]}. \tag{12}$$

The voltage across the resonant capacitor C_r attempts next the negative swing. However, the antiparallel diode turns-on and re-routes the current flow until the energy is discharged. During this interval, the voltage across the L_r is maintained constant and equal to converter's input voltage. A constant voltage drop across L_r means a linear variation:

$$i_{DSw}(t) = i_{Lr}(t) = \left[-I_L\sqrt{\left[1-\left[\frac{E}{Z_r I_L}\right]^2\right]}\right] + \frac{E}{L_r}(t-t_2). \tag{13}$$

The current through the output diode D results as:

$$i_D(t) = I_L\left[1+\sqrt{\left[1-\left[\frac{E}{Z_r I_L}\right]^2\right]}\right] + \frac{E}{L_r}(t-t_2). \tag{14}$$

The main switch should not be turned-on before all energy vanishes. The moment of time t_3 when the current through the resonant inductor and the anti-parallel diode reaches zero is:

$$t_3 = t_2 + \frac{1}{\omega_r}\cdot\frac{Z_r I_r}{E}\sqrt{\left[1-\left[\frac{E}{Z_r I_L}\right]^2\right]}. \tag{15}$$

For an economical operation, the OFF state of the switch needs to match the time interval between t_1 and t_3. A turn-on command for the main switch produces a current circulation through *Sw*, the resonant inductor L_r and the output diode. Because the output diode is still in the ON state, the voltage across the resonant inductor equals the input voltage $\boldsymbol{E}$. The main switch current will continue the linear variation from zero to the load current I_L.

$$i_D(t) = I_L\left[1+\sqrt{\left[1-\left[\frac{E}{Z_r I_L}\right]^2\right]}\right]+\frac{E}{L_r}\left(t-t_2\right). \tag{16}$$

The output diode current will eventually reach zero at t_4.

$$t_4 = t_3+\frac{1}{\omega_r}\cdot\frac{Z_r I_r}{E} = t_2+\frac{1}{\omega_r}\cdot\frac{Z_r I_r}{E}\left[1+\sqrt{\left[1-\left[\frac{E}{Z_r I_L}\right]^2\right]}\right]. \tag{17}$$

After the moment t_4, the switch is the only device carrying current towards the load through the resonant inductor L_r. The main switch can be turned-off at any time and the entire operation cycle repeated. Fig. 2 illustrates the critical time intervals for the resonant operation. Instants t_2 and t_4 are very important because they limit the possible variation of the ON and OFF time intervals within the controller operation. Their values are dependent on L_r and C_r as well as on the load current and converter's input voltage. In most design and analysis circumstances, the passive components can be considered as having constant parameters and the load current becomes the only variable parameter during the operation of the power stage. This guarantees a proper operation of the resonant circuit when the following constraint is respected.

$$Z_r \cdot I_L \geq E. \tag{18}$$

This means:

• The *Zero Voltage Transition (ZVT)* can be obtained for certain current levels and that light loads do not concur to reduction of the switching loss.

• Since the duration of the off-state is dictated by the circuit conditions, the resonant buck converter can control the output voltage only by changing the period of the entire cycle. Obviously, equation (18) allows a multitude of design options. We have adopted herein a design guaranteeing for a resonant operation at any current above 40% of the maximum load current:

$$\sqrt{\frac{L_r}{C_r}}0.4I_L \geq E. \tag{19}$$

The average output voltage can be calculated by:

$$V_{\text{out}} = E\left[1-\frac{t_{\text{zero}}}{T}\right]+E\frac{1}{2}\cdot\frac{E}{I_L}\cdot\frac{1}{\omega_r Z_r}, \tag{20}$$

where

$$t_{\text{zero}} = t_4-t_0 = \frac{E}{I_L}\cdot\frac{1}{\omega_r Z_r}+\frac{1}{\omega_r}\left[\pi+\arcsin\left(\frac{E}{Z_r I_L}\right)\right]+ \\ +\frac{1}{\omega_r}\cdot\frac{Z_r I_r}{E}\left[1+\sqrt{\left[1-\left[\frac{E}{Z_r I_L}\right]^2\right]}\right]. \tag{21}$$

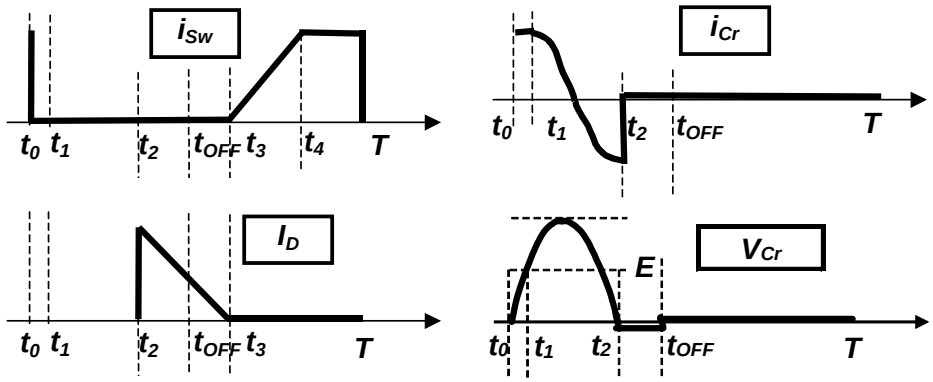

Fig. 2 – Important moments for operation of the Resonant Buck Converter.

For a numerical example, a buck converter with data from Table 1 has been considered. It yields:

$$\frac{L_r}{C_r} \geq 225 \rightarrow L_r = 5\ \mu\text{H};\ C_r = 22\ \text{nF}. \tag{22}$$

Table 1

System Data

MOSFET Transistor IRF460
Gate voltage = 20 V
Gate resistance = 4.3 Ohm
Switching frequency 198 kHz
Duty cycle for operation at 20 A, 66%
Ambient temperature = 280C
Power Diode CS240650
Supply voltage 120 V
Output voltage 48 V (potentual telecom application)
Variable load current

The output voltage decreases with resonant operation, and requires a wider duty cycle in order to achieve the same output voltage. Otherwise, the further the design is from loss of resonance property, the lower the output voltage results at the same duty cycle. Using a wider duty cycle means one trades switching loss for conduction loss. Table 2 illustrates the variation of the output voltage at 0 to 25% variation of parameters *Lr*, *Cr* for the numerical example previously considered. Contrary to the case of a conventional buck converter, the resonant buck converter produces an output voltage dependent on the circuit parameters (see equation 20). The only control lever is the period of the entire operational cycle, herein denoted with *T*. Most contemporary design strategies consider constant values for the parameters L_r and C_r, and discuss the possible variation of the output voltage with load current and input voltage.

Feed-forward alteration of the control decision or direct measurement of the transition moments complete the actual control system for such cases.

Table 2

Variation of the Output Voltage with Resonant Parameter Variation, for the Numerical Data Set From Table 1, Calculated for Ideal Conditions of Neglecting Caloric (Resistive) Loss and Voltage Drop Across Power Semiconductor Components, and for a Constant Switching Frequency at Each Current

Cr[nF]\ Lr[uH]	3.75	4.00	4.25	4.50	4.75	5.00	5.25	5.50	5.75	6.00	6.25
16.50	68.19	65.60	63.03	60.48	57.94	55.42	52.91	50.41	47.93	45.46	42.99
17.60	67.34	64.73	62.15	59.57	57.02	54.48	51.95	49.44	46.94	44.45	41.97
18.70	66.51	63.89	61.28	58.69	56.12	53.56	51.02	48.49	45.97	43.47	40.97
19.80	65.70	63.06	60.43	57.83	55.24	52.66	50.10	47.56	45.02	42.50	39.99
20.90	64.91	62.24	59.60	56.98	54.37	51.78	49.21	46.65	44.10	41.56	39.04
22.00	64.13	61.44	58.79	56.14	53.52	50.92	48.33	45.75	43.19	40.64	38.10
23.10	63.36	60.66	57.98	55.33	52.69	50.07	47.46	44.87	42.30	39.73	37.18
24.20	62.60	59.89	57.20	54.52	51.87	49.23	46.61	44.01	41.42	38.84	36.27
25.30	61.86	59.13	56.42	53.73	51.06	48.41	45.78	43.16	30.55	37.96	35.38
26.40	61.13	58.38	55.65	52.95	50.27	47.60	44.96	42.32	39.70	37.10	34.51
27.50	60.40	57.64	54.90	52.18	49.49	46.41	44.14	41.50	38.87	36.25	33.65

(a) Output voltage in [V] for ideal operation at maximum load current of 20 A, switching frequency 198 kHz.

Cr[nF]\ Lr[uH]	3.75	4.00	4.25	4.50	4.75	5.00	5.25	5.50	5.75	6.00	6.25
16.50	67.17	64.93	62.72	60.53	58.36	56.20	54.06	51.94	49.83	47.74	45.65
17.60	65.90	63.64	61.41	59.20	57.00	54.83	52.67	50.52	48.39	46.28	44.17
18.70	64.66	62.38	60.12	57.89	55.67	53.47	51.30	49.13	46.98	44.85	42.73
19.80	63.44	61.13	60.86	56.60	54.36	52.15	49.95	47.76	45.60	43.44	41.30
20.90	62.23	59.91	58.61	55.33	53.08	50.84	48.62	46.42	44.24	42.06	39.91
22.00	61.04	58.70	57.38	54.09	51.81	49.56	47.32	45.10	42.90	40.71	38.53
23.10	59.87	57.51	55.17	52.86	50.56	48.29	46.03	43.80	41.58	39.37	37.18
24.20	58.71	56.33	53.97	51.64	49.33	47.04	44.77	42.51	40.27	38.05	35.84
25.30	57.57	55.17	52.79	50.44	48.11	45.80	43.51	41.24	38.99	36.75	34.53
26.40	56.41	54.01	51.62	49.25	46.91	44.58	42.28	39.99	37.72	35.47	33.23
27.50	55.31	52.87	50.46	48.08	45.72	43.38	41.06	38.75	36.47	34.20	31.95

(b) Output voltage in [V] for ideal operation at a load current of 12 A (60%), switching frequency 247 kHz.

The experimental setup delivers 48 V for ideal constraints. Obviously, operation within a closed-loop control system would adjust the switching frequency to account for these variations in order to keep the output voltage constant. Since 1986, interest in resonant mode power conversion has sparked and a series of control ICs have been introduced on the market. A list includes LD405, GP605, CS3805, UC3860, UC1861, UC1864, UC1865, MC34066, and CS360. These all share a common operational philosophy: fixed-pulse-width variable-frequency. Analogously, digital implementation has been considered.

Table 3 checks for the resonant system constraint when a closed-loop system forces the output voltage at reference value for cases considered in

Table 2. It can be seen that ± 25% variation of the parameters produces a variation of the control period within the same range. This may not be allowed sometimes.

Table 3
Variation of the Switching Period (in Seconds), with Parameter Values of the Resonant Circuit in Order to Keep the Output Voltage Constant Under a Load Current of 20 A.

Cr\Lr	3.75	4.50	5.00	5.50	6.25
16.50	3.876E-06	4.464E-06	4.785E-06	5.208E-06	5.747E-06
19.80	4.016E-06	4.608E-06	4.975E-06	5.405E-06	6.024E-06
22.00	4.098E-06	4.739E-06	5.128E-06	5.525E-06	6.061E-06
24.20	4.237E-06	4.878E-06	5.236E-06	5.650E-06	6.211E-06
27.50	4.348E-06	4.975E-06	5.405E-06	5.780E-06	6.410E-06

3. Ageing and After-Shock Parameter Variation for the Passive Components

This article considers ageing and after-shock parameter variation for the passive components as a possible deterioration of the resonant constraint. As a mostly neglected secondary effect, these also deteriorate the reliability performance and reduce the lifetime of the converter. A series of recent research reports (Overton *et al.*, 1993, Kindmark & Rosen, 2013) have addressed the problem of parameter variation due to ageing or operation after-shock. Ageing is a normal process of using the passive components continuously, under nominal conditions. The most noticeable effect of ageing in passive components consists of the increase of calorimetric (resistive) loss. However, certain technologies for passive components fabrication are demonstrated to produce slight variation of the nominal values of the main parameter, either inductance or capacitance. A similar effect, rather difficult to demonstrate experimentally, consists in a change of the main parameter (inductance, capacitance) due to an operational shock. If the inductor's current or the capacitor's voltage is occasionally reaching an unexpectedly high value, this may have remanence effect on the value of the main parameter. Without approaching a complete quantification of such effects, this article takes them into account and estimates the effect of an inadequate value of inductance or capacitance to the resonant circuit in a resonant buck converter. While a conventional filter application may not be that affected by a 10% change in inductance or capacitance values, such change would produce a mis-alignment of the control pulses in the case of a resonant buck converter. This may add up to other similar effects derived from a digitization under a digital control platform or errors in sensing and measurement system.

4. Operation with Mis-Alignment of the Control Pulse

Fig. 3 illustrates the operation of the power switch near the ideal case, with reduced switching loss due to zero voltage transition of the main switch.

The duty cycle or the pulse frequency could be even better adjusted for a switching of the power device when the capacitor current approaches zero.

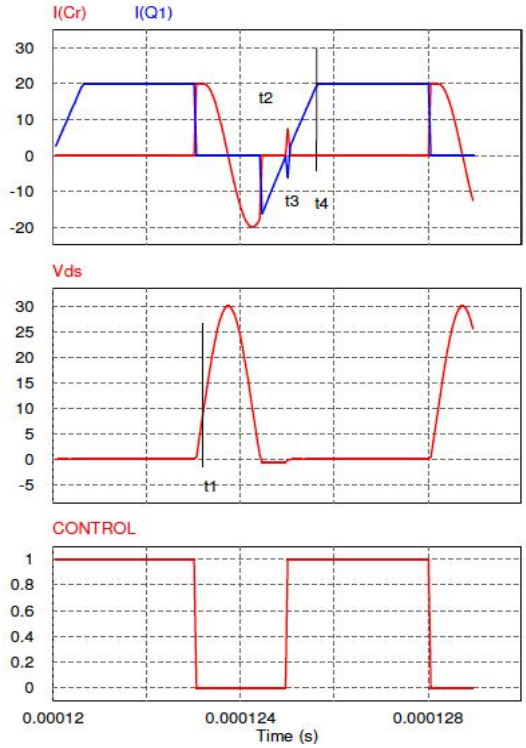

Fig. 3 – Illustration by circuit simulation of the proper operation of the switch for Zero Transition Switching. NoteVin = 10 V and I_L = 20 A.

Fig. 4 shows results for the same circuit, when a slight change in the inductance value has occurred. This may be due to either thermal effects, negligence in design or stockroom supply, or repeated operation of the magnetic device at its extreme limits, near saturation, with remanence effects. It can be noticed that the resonant circuit swings more and the power switch needs to support both the load current and the instantaneous discharge of the capacitor. Since the turn-on current is larger, an additional power loss occurs. The temperature of both the device and introduced passive components increases.

For a complete comparison, Fig. 5 shows waveforms for a conventional buck circuit. Since the reliability strongly depends on the operational temperature of the power semiconductor devices, a precise evaluation of power loss and temperature is required. There are two methods for a comprehensive analysis of the parameter implications on power loss and temperature:

- A high-level simulation model for the power semiconductor device associated with a systematic parameter variation (Oeder *et al.*, 2016).
- A thermal camera monitoring of the system when parameters are changed, under a test duration time penalty (Butnicu, 2019).

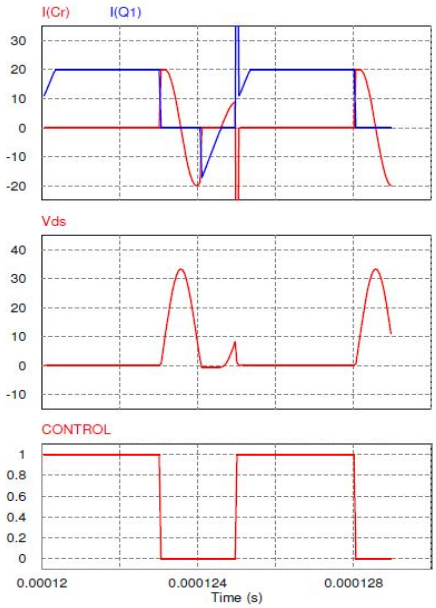

Fig. 4 – Illustration by circuit simulation of the delayed control due to mis-alignment of the control pulse and resonant swing. Note Vin = 10 V and I_L = 20 A.

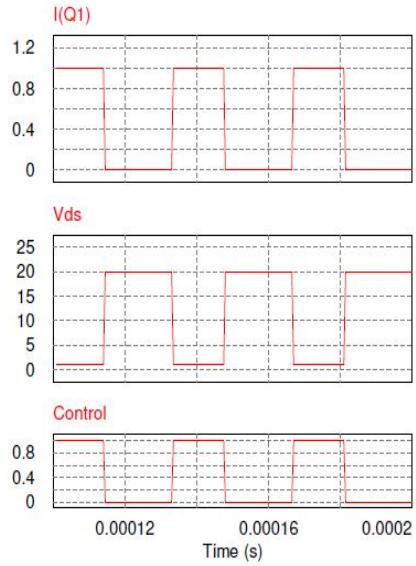

Fig. 5 – Switching within the conventional buck converter.

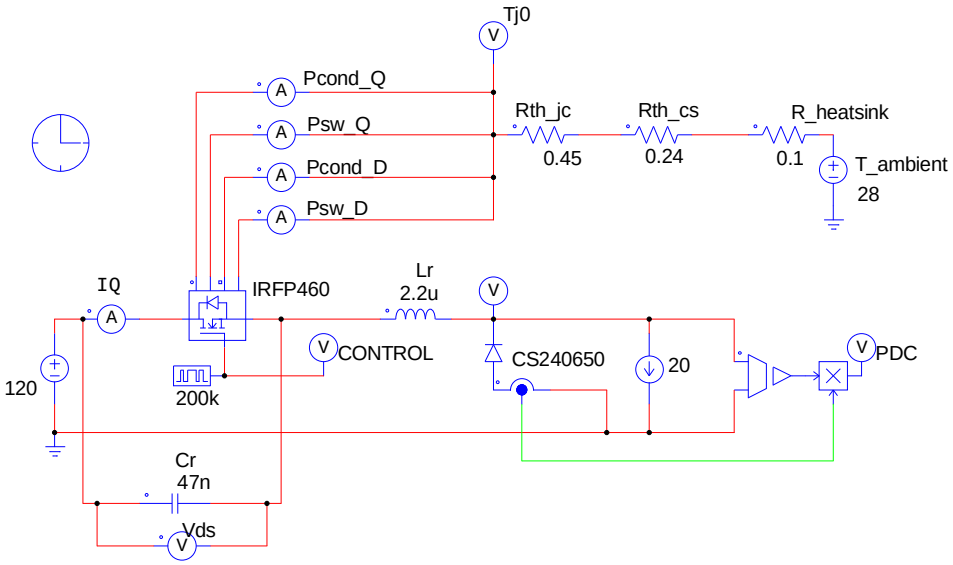

Fig. 6 – Simulation based analysis for the thermal effects of parameter variation.

Over the last decade, simulation models have been improved and high-level models are now available with loss components, in both PSIM and PSPICE. While a level-1 model limits to the study of an ideal switch, a level-3 model includes all parasitic components in the model. Hours of analysis at various operation points can be saved. The goal of a simulation-based test is to prove and quantify the thermal effects of an operation with mis-alignment due to resonant component variation. This test follows the simulation-based procedure described in (Oeder *et al.*, 2016). While (Oeder *et al.*, 2016) considers the effect of each parameter on the reliability calculation, this article considers a dataset of constant parameters during the test with just a variation of the passive resonant components.

A PSIM thermal model for IRF460 MOSFET transistor is considered in Fig. 6. A Powerex CS240650 diode completes the buck converter setup. The power MOSFET model defines power loss components based on datasheet information embedded within the PSIM model. This means power components are compiled from graphs based on E_{ON} and E_{OFF} energies, rather than calculated as a current-voltage product. The static junction temperature value is calculated externally, as shown. Tests are performed at a nominal load current of 20 A and tabled for variation of the inductance and capacitance values, from nominal to a maximum of ±25%. While methods for limitation of the switching period range exist, Table 4 shows the junction temperature change when the control period is maintained within a variation range of ±10%.

Table 4

Junction Temperature (measured in Celsius) when the Control Period is Limited Within the Range 4.80 μsec to 5.30 μsec, with a Constant Output Voltage and Under a Load Current of 20 A. Region with the Truncated Operational Period is Hatched. The Thermal Model for the Transistor Includes Rth_jc = 0.45°C/W, Rth_cs = 0.24°C /W, Rth_Heatsink = 0.10 °C /W and Ambient Temperature of 28°C.

Cr|Lr	3.75	4.50	5.00	5.50	6.25
16.50	**173.00**	115.00	104.64	110.71	97.81
19.80	132.95	108.45	102.80	104.52	92.24
22.00	122.85	104.43	102.30	100.84	89.91
24.20	117.70	97.50	102.14	97.44	85.89
27.50	111.86	99.99	101.34	92.76	81.56

5. Reliability Calculation

As the circuit topologies have been established and their ideal performance understood, the researchers focused on assessment of the reliability and lifetime performance. The failure rate of a system is calculated from the failure rates for each individual component. For the case of power converters, all components are considered equally important. This means that the components are considered as being "in series" within the system. In a series system that includes *n* components, the overall failure rate:

$$\lambda_{\text{SYSTEM}} = \sum_{i=1}^{N} \lambda_i, \tag{23}$$

where: λ_i corresponds to the individual failure rates of the components, like power semiconductor devices, capacitors or inductors. For the resonant buck converter, the failure rate yields:

$$\lambda_{\text{SYSTEM}} = \lambda_{\text{MOSFET}} + \lambda_{\text{CONTROL}} + \lambda_{\text{DIODE}} + \lambda_{\text{INDUCTOR}} + \lambda_{\text{OUT\_CAPACITOR}} + \\ + \lambda_{Lr} + \lambda_{Cr}. \tag{24}$$

Even for components manufactured under identical conditions, the failure rates can vary by a factor of 10 depending on the conditions under which the device is used. This means that the system failure rate is herein not only influenced by addition of two new terms ($\lambda_{Lr} + \lambda_{Cr}$), but also by different values for components present in both conventional and resonant buck converters, due to their different operation point. Each individual component (or term in equation 21) is considered to have a constant failure rate (λ_{base}), which is further de-rated through a series of stress factors depending on manufacturing, environmental, and circuit use of devices

$$\lambda = \lambda_{\text{base}} \prod_{i=1}^{m} \pi_i = \lambda_{\text{base}} \pi_T \pi_S \pi_A \pi_R \pi_E \pi_C \pi_Q. \tag{25}$$

The stress factors (λ_i) refer to temperature, voltage stress, circuit/ application, rating, environment, construction factor, and product quality, respectively. Some of these stress factors have similar values for conventional and resonant converters, some are different due to their different operation points. The way these stress factors are calculated or defined comes from the particular method used for calculation. The most commonly used methods for reliability calculation from circuit data are MIL-HDBK-217, TR62380 and FIDES. MIL-HDBK-217 is decisively the most frequently used method. It is an older US military standard with data based on a wide collection of results. Unfortunately, it does not provide too much detail on the new technologies for inductors and capacitors (Butnicu, 2019).

IEC TR62380 is presented by the International Electrotechnical Commission. The drawback of this standard consists of a minimal dependence on temperature. In (Riedel *et al*., 2012; Valipour *et al*., 2015) the dependence of the reliability calculations of different standards on the temperature has been analyzed and it has been shown that the temperature has a little influence on calculations in IEC TR62380 and a great dependency on the temperature in FIDES and MIL-HDBK-217 based calculations. For this reason, the failure rate calculated with this standard usually produces of a lower value than MIL-HDBK-217.

Finally, the FIDES method shows no dependence of the semiconductor reliability on the voltage stress. In most cases, this does not matter since the circuit designers always consider the applied voltage far enough from the nominal voltage. This would also be the case with the resonant buck converter. A conventional MIL-HDBK-217 calculation has been considered for the analysis in this article.

Another standard, not used herein, is Siemens SN 29500.

Previously, the same approach has been used in (Valipour, 2014) for a comparison between a typical hard switching converter and an LLC soft switching converter. It had demonstrated that the lifetime of the soft switching converter is much greater than the reliability of the hard switching circuit in close to ideal operational conditions. However, the very same reference suggested to continue the investigations on parameter variations and mis-alignment.

A comparative calculation is performed in this paper, for three cases, under 20A load and 48V output voltage.

- Ideal resonant converter, without limitation of the switching frequency range, leading to around 100°C for the MOSFET junction temperature, and a dissipated power of 11.8W on the buck diode.
- A converter with 10% limit of frequency range, leading to results from Table 4 and a maximum MOSFET junction temperature of 173°C, and a maximum dissipated power on the buck diode of 9.6W.
- A conventional non-resonant buck converter, operated under the same input-output conditions, and leading to operation with MOSFET junction temperature of 109°C, and a dissipated power on buck diode of 10.2W.

The control circuit and the main passive components (buck inductor and the output capacitor) can be considered with the same failure rate for the three circuits. Our comparison restricts itself to the main power semiconductor devices (MOSFET) and the added resonant components. The system-level failure rate for the three cases result as follows

$$\Delta\lambda_1 = \lambda_{\text{MOSFET},1} + \lambda_{\text{DIODE},1} + \lambda_{Lr,1} + \lambda_{Cr,1}, \tag{26}$$

$$\Delta\lambda_2 = \lambda_{\text{MOSFET},2} + \lambda_{\text{DIODE},2} + \lambda_{Lr,2} + \lambda_{Cr,2}, \tag{27}$$

$$\Delta\lambda_3 = \lambda_{\text{MOSFET},3} + \lambda_{\text{DIODE},3}. \tag{28}$$

The main power MOSFET device has a failure rate as follows.

$$\lambda_{\text{MOSFET}} = \lambda_{\text{base}}\pi_A\pi_T\pi_V\pi_Q\pi_E. \tag{29}$$

As per MIL-HDBK-217F (notice 2 of February 28th, 1995), the base failure rate for a low-frequency Si FET (page 6.8/61) is 0.012.

The stress factors (π) refer to temperature, voltage stress, circuit/application, rating, environment, construction factor, and product quality, respectively. The stress factors depend on application and can be identified for each of the three cases selected for our analysis as being the same except for the temperature.

- Application factor π_A = 10, for power levels above 250 W.
- Environment factor π_E = 6, for application classified as "*Ground, Fixed*" (Moderately controlled environments such as installation in permanent racks with adequate cooling air and possible installation in unheated buildings, like the usage of communication equipment).
- Quality factor π_Q = 2.4, production of discrete semiconductors ("*JAN*").
- Voltage factor is considered as unitary.
- Temperature factor π_T depends strongly on temperature within a ratio of 1:8.7. For the example in Table 1, consider just the highest temperature, that is coming from operation at 20 A. Thus, the temperature factor equals 3.7 for 100°C, 8.7 for 173°C, and 4.2 for 109°C, respectively.

FIT is preferred for measurement of failure rate, as per JEDEC JESD85, which is a standard used for semiconductors and thus relevant for most electronics.

This means:

$$\lambda_{\text{MOSFET},1} = \lambda_{\text{base}}\pi_A\pi_T\pi_V\pi_Q\pi_E = 0.012\times10\times6\times2.4\times1\times3.7 = \\ = \frac{6.39F}{10^6 h} = 6,390\text{FIT}, \tag{30}$$

$$\lambda_{\text{MOSFET},2} = \lambda_{\text{base}}\pi_A\pi_T\pi_V\pi_Q\pi_E = 0.012\times10\times6\times2.4\times1\times8.7 = \\ = \frac{15.03F}{10^6 h} = 15,030\text{FIT}, \tag{31}$$

$$\lambda_{\text{MOSFET},3} = \lambda_{\text{base}}\pi_A\pi_T\pi_V\pi_Q\pi_E = 0.012\times10\times6\times2.4\times1\times4.2 = \\ = \frac{7.25F}{10^6 h} = 7,250\text{FIT}. \tag{32}$$

A power Si diode has a failure rate as follows

$$\lambda_{\text{DIODE}} = \lambda_{\text{base}}\pi_C\pi_T\pi_V\pi_Q\pi_E. \tag{33}$$

As per MIL-HDBK-217F, the base failure rate for a low-frequency fast-recovery Si diode (Page 6.1/55) is 0.025. The power dissipated on the buck diode is varying within the range 9.6W to 11.2W, as explained. The stress factors depend on application and can be identified for each of the three cases selected for our analysis as being the same except for the temperature.

- Construction factor $\pi_A = 1$.
- Environment factor $\pi_E = 6$, for application classified as "Ground, Fixed" (Moderately controlled environments such as installation in permanent racks with adequate cooling air and possible installation in unheated buildings, like the usage of communication equipment).
- Quality factor $\pi_Q = 2.4$ production of discrete semiconductors ("JAN").
- Voltage factor is considered as unitary.
- Temperature factor $\pi_T = 1.9$ is considered for a temperature of around 44°C, expressed by a limited variation range during operation (between 38 and 46°C).

This means the lifetime for any of the three cases is almost equal to:

$$\lambda_{\text{DIODE 1,2,3}} = \lambda_{\text{base}}\pi_C\pi_T\pi_V\pi_Q\pi_E = 0.025\times1\times6\times2.4\times1\times1.9 = \\ = \frac{0.684F}{10^6 h} = 684\text{FIT}. \tag{34}$$

The resonant capacitor contributes to the failure rate.

$$\lambda_{C\text{ceramic}} = \lambda_b \pi_Q \pi_E \pi_{\text{CV}} = 0.00075 \times 1 \times 10 \times 2 = 0.015 \text{ F}/10^6\text{h} = 15 \text{ FIT}. \tag{35}$$

The resonant inductor contributes to the failure rate.

$$\lambda_L = \lambda_b \pi_Q \pi_E \pi_{\text{CV}} = 0.00075 \times 1 \times 10 \times 3 = 0.015 \text{ F}/10^6\text{h} = 22.5 \text{ FIT}. \tag{36}$$

Finally, system-level failure rates for the three cases are graphically shown within Fig. 7 as they result from the following calculation:

$$\Delta\lambda_1 = \lambda_{\text{MOSFET},1} + \lambda_{\text{DIODE},1} + \lambda_{Lr,1} + \lambda_{Cr,1} = 639 + 69 + 2 + 3 = 7,111 \text{ FIT}, \tag{37}$$

$$\Delta\lambda_2 = \lambda_{\text{MOSFET},2} + \lambda_{\text{DIODE},2} + \lambda_{Lr,2} + \lambda_{Cr,2} = 1,503 + 69 + 2 + 3 = 15,751 \text{ FIT}, \tag{38}$$

$$\Delta\lambda_3 = \lambda_{\text{MOSFET},3} + \lambda_{\text{DIODE},3} = 725 + 69 = 7,319 \text{ FIT}. \tag{39}$$

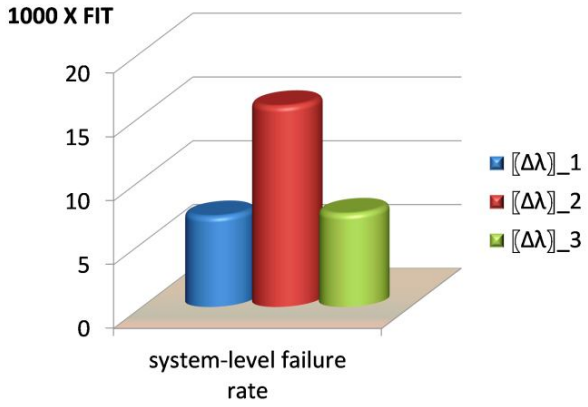

Fig. 7 – System-level failure rate for the three cases.

6. Conclusion

This paper studies the effect of parameter variation for a ZVS resonant buck converter. This converter keeps the output voltage constant with a variation of the switching frequency. Since the allowed switching period variation may be limited in hardware to a ±10% range, certain sets of values lead to undesired junction temperature rise. Consequently, this produces a deterioration of the reliability and lifetime. A dataset is considered as example and a full estimation of reliability performance is presented based on MIL-HBK-217F for several cases. It is concluded that parameter variation must be fully understood and taken into consideration during the design phase. Otherwise a deterioration of reliability performance results.

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DESPRE DEGRADAREA PERFORMAŢEI DE FIABILITATE DATORITĂ PIERDERII SINCRONIZĂRII LA CONVERTOARELE REZONANTE ZVT

(Rezumat)

Convertoarele rezonante de putere se folosesc într-o gamă largă de aplicații datorită avantajelor legate de reducerea pierderilor în comutație. Totuşi, controlul acestor convertoare necesită o adaptare continuă a momentelor de comutație în funcție de sarcină, de tensiunea de alimentare sau la schimbarea parametrilor circuitului resonant. Dacă circuitul rezonant este comutat înainte sau după ce tranziția rezonantă are loc, pierderile de putere cresc, temperatura joncțiunii creşte, şi fiabilitatea este influențată negativ. Acest articol analizează această problemă pentru cazul particular al unui convertor rezonant ZVT (cu comutație la tensiune nulă) şi estimează efectele pierderii sincronizării momentelor de control asupra fiabilității.