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A NEW VLSI ALGORITHM FOR A VLSI IMPLEMENTATION OF TYPE IV DST WITH LOW HARDWARE COMPLEXITY

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Abstract. A new VLSI algorithm for a VLSI implementation with a low hardware complexity of type IV DST using only a single band correlation structure is presented. This approach is based on a new systolic array algorithm that uses an efficient restructuring of the type IV DST computation into a regular and modular computational structure called band-correlation. The proposed algorithm can be efficiently mapped into a linear systolic array having a small number of I/O channels with a low I/O bandwidth and a low hardware complexity. The systolic array that can be thus obtained have all the advantages of the systolic arrays based on circular correlation structure as a good architectural topology, with small and local interconnection structure, modularity and regularity and also a high processing speed.

Keywords: discrete transforms; discrete sine transforms; systolic arrays; systolic algorithms; VLSI algorithms.

1. Introduction

The type IV DCT and DST belongs to the discrete cosine transform (DCT) and discrete sine transform (DST) family and are basic functions in many signal processing applications, especially in speech and image transform coding. DCT offers good results for highly correlated signals and DST provides lower bit rates for low-correlated signals. DCT was first introduced in 1974

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(Ahmed *et al*., 1974) and since then, other four DCTs, namely, DCT-I,DCT-II,DCT-III and DCT-IV have been developed (Jain, 1979). Also four other DSTs, namely DST-I,DST-II,DST-III and DST-IV, have also been introduced.

Type IV DCT and DST (DCT-IV and DST-IV) are related to generalized Fourier transform (GDFT) and generalized discrete Hartley transform (GDHT) for real data sequences. They can be used in the fast implementation of lapped orthogonal transforms, in signal and image coding (Jing *et al*., 2001; Malvar, 1990, 1991), perfect reconstruction cosine-modulated filter banks (Chan, 2000) and are also used in Dolby Labs AC-3 digital audio compression algorithm.

Until now, just a few solutions of an efficient hardware implementation for type IV DST have been presented (Kidamni, 1998; Chiper, 2013).

Data flow is important for an efficient VLSI implementation, even more important than computational complexity. This is one of the reasons why some computational structures as circular correlation and cycle convolutions are so important in obtaining an efficient VLSI implementation using systolic arrays (Kung, 1982) and distributed arithmetic (White, 1989).

This paper presents the use of another computational structure that is modular and regular and can be efficiently implemented in VLSI using the systolic arrays architectural paradigm, called pseudo band-correlation, leading to an efficient VLSI implementation with a low hardware complexity.

The presented method introduces a decomposition of the type IV DST (DST-IV), using a single pseudo-band correlation which leads to an efficient hardware implementation that is based on the architectural paradigm of systolic arrays. The reformulated algorithm introduces some auxiliary sequences and is using the Galois Fields of indexes properties. The achieved decomposition shows a single computational structure that is simplified from a computational perspective and thus a significant reduction of the hardware complexity is obtained.

2. A VLSI Algorithm for 1-D DST IV Based on Pseudo-Band Correlation Structures

For the real input sequence $x(i): i = 0,1,...,N-1$, 1-D type IV DST (DST-IV) is defined as:

$$Y(k) = \sqrt{\frac{2}{N}} \sum_{i=0}^{N-1} x(i) \sin[(2i+1)(2k+1)\alpha]; \quad k = 0,1,\ldots,N-1, \qquad (1)$$

where: $\alpha = \pi / 4N$.

In the derivation of the new algorithm, we can drop the constant coefficient $\sqrt{2/N}$ from equation (1). Then at the end of the obtained architecture we will add a multiplier to scale the output sequence with this constant.

In order to derive the new algorithm it was necessary to recast relation (1) as a pseudo-band correlation form. In order to do this we have introduced some auxiliary input and output sequences and we have permuted the input and output samples using the proprieties of the Finite Field of indexes.

$$Y(0) = x_a(0) * \sin(\alpha) + 2T_a(0) * \cos(\alpha), \tag{2}$$

$$Y(1) = x_a(0) * \sin(3\alpha) + 2T_a(1) * \cos(3\alpha), \tag{3}$$

$$Y(2) = x_a(0) * \sin(5\alpha) + 2T_a(2) * \cos(5\alpha), \tag{4}$$

$$Y(3) = x_a(0) * \sin(7\alpha) + 2T_a(3) * \cos(7\alpha), \tag{5}$$

$$Y(4) = x_a(0) * \sin(9\alpha) + 2T_a(4) * \cos(9\alpha), \tag{6}$$

$$Y(5) = x_a(0) * \sin(11\alpha) + 2T_a(5) * \cos(11\alpha), \tag{7}$$

$$Y(6) = x_a(0) * \sin(13\alpha) + 2T_a(6) * \cos(13\alpha), \tag{8}$$

where the input auxiliary sequence $\{x_a(i) : i = 0,...,N-1\}$ is recursively computed as following:

$$x_a(N-1) = x(N-1), \tag{9}$$

$$x_a(i) = x(i) + x_a(i+1), \text{ for } i = N-2,\ldots,0, \tag{10}$$

and the auxiliary output sequence $\{T_a(k) : k = 1,2,...,N-1\}$ can be recursively computed as follows:

$$T_a(0) = \sum_{i=0}^{N-1} x_a(i)\sin(2i\alpha) = \sum_{i=0}^{N-1} x_S(i), \tag{11}$$

$$T_a(k) = T_S(k) - T_a(k-1), \text{ for } k = 1, 2,\ldots, N-1, \tag{12}$$

with the auxiliary input sequences $x_C(i)$ and $x_S(i)$ computed as:

$$x_C(0) = x_a(0) * \cos(0 \times \alpha), \tag{13}$$

$$x_C(1) = x_a(1) * \cos(2 \times \alpha), \tag{14}$$

$$x_C(2) = x_a(2) * \cos(4 \times \alpha), \tag{15}$$

$$x_C(3) = x_a(i) * \cos(6 \times \alpha), \tag{16}$$

$$x_C(4) = x_a(i) * \cos(8 \times \alpha), \tag{17}$$

$$x_C(5) = x_a(i) * \cos(10 \times \alpha), \tag{18}$$

$$x_C(6) = x_a(i) * \cos(12 \times \alpha), \tag{19}$$

and

$$x_S(0) = x_a(0) * \sin(0 \times \alpha), \tag{20}$$
$$x_S(1) = x_a(1) * \sin(2 \times \alpha), \tag{21}$$
$$x_S(2) = x_a(2) * \sin(4 \times \alpha), \tag{22}$$
$$x_S(3) = x_a(3) * \sin(6 \times \alpha), \tag{23}$$
$$x_S(4) = x_a(4) * \sin(8 \times \alpha), \tag{24}$$
$$x_S(5) = x_a(5) * \sin(10 \times \alpha), \tag{25}$$
$$x_S(6) = x_a(6) * \sin(12 \times \alpha). \tag{26}$$

The auxiliary output sequence $\{T_S(k) : k = 1,2,...,N-1\}$ can be computed as follows:

$$\begin{bmatrix} T_S(4) \\ T_S(2) \\ T_S(6) \\ T_S(3) \\ T_S(5) \\ T_S(1) \end{bmatrix} = \begin{bmatrix} -s(2) & -s(6) & -s(4) \\ s(6) & s(4) & -s(5) \\ s(4) & -s(5) & -s(1) \\ -s(5) & s(1) & s(3) \\ s(1) & -s(3) & s(2) \\ -s(3) & s(2) & s(6) \end{bmatrix} \cdot \begin{bmatrix} x_C(3) \pm x_C(4) \\ x_C(3) \pm x_C(4) \\ x_C(3) \pm x_C(4) \end{bmatrix}. \tag{27}$$

For the first three terms $T_S(4), T_S(2)$ and $T_S(6)$ we are considering the minus operation for $x_C(i) \pm x_C(N-i)$ and for the next three terms $T_S(3), T_S(5)$ and $T_S(1)$ we are considering the plus operation.

We have used

$$s(i) = 2 \cdot \sin(i \cdot 2\alpha) \tag{28}$$

and some permutations of the indexes given by:

$$\varphi(k) = < g^K >_N, \tag{29}$$

where we have used the properties of the Finite Fields with the primitive root $g = 3$ and $N = 7$.

From equation (27) we can see that all the elements along the secondary diagonal of the matrix in (27) are the same and all the elements on the lines parallel with this secondary diagonal are also the same as shown in Fig. 1. We'll call this regular computational structure band-correlation. As there are some differences in sign this computational structure will be called pseudo band-correlation structure.

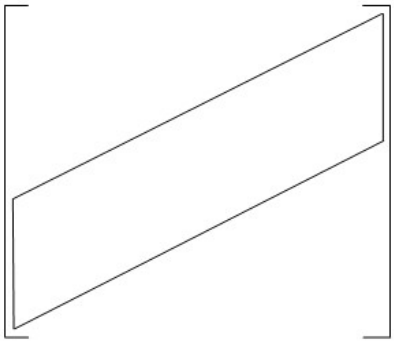

Fig. 1 – The structure of the computational structure called pseudo-band correlation.

The signs of terms in relation (27) the sign of the elements along the secondary diagonal are different and are given by the functions $\varepsilon(k,i)$ that is defined bellow

$$\varepsilon(k,i) \text{ is given by } \begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 1 \\ 0 & 1 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix}$$

where 1 coresponds to minus sign and 0 to the plus sign.

3. A VLSI Implementation Discussion

In order to obtain the VLSI architecture we are using the previous algorithm and an appropriate synthesis procedure. Thus, it is possible to derive an efficient VLSI architecture using the systolic array paradigm. Using the dependence-graph based procedure (Kung, 1988) we can map equation (27) onto a single linear systolic array having 3 processing elements that are working in a pipeline manner. This systolic array represents the hardware core of the architecture used for the VLSI implementation of the proposed algorithm.

Each processing element contains a multiplier, an adder and a multiplexer. The multiplexer can select the proper input data to be used in each multiplier.

Using an appropriate control mechanism that is using tag control bits (Jen *et al.*, 1988) we can control the input data in that is used in each PE so that all the input and output channels to be placed at one of the two ends of the linear systolic array.

This architecture offers a high processing speed by using pipelining. The high data rate inside the array will contribute to a high volume of data to be input to the systolic array. It is the so called I/O bottleneck that will reduce the speed performances of a pipeline architecture. In our solution the so-called I/O bottleneck is avoided by using each data in many PE as much as possible.

4. Conclusions

In this paper a new VLSI algorithm for type IV DST VLSI implementation with a low hardware complexity is presented. The proposed VLSI algorithm has been obtained using an appropriate reformulation of type IV DST into a single modular and regular computational structure called pseudo band correlation. The proposed algorithm can be efficiently mapped onto a single linear systolic array having a small number of I/O channels with a low I/O bandwidth and have all the advantages of the systolic array implementations that uses circular correlation as a good architectural topology, with small and local interconnection structure, modularity and regularity and also a high processing speed.

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UN NOU ALGORITM VLSI PENTRU IMPLEMENTAREA HARDWARE A TRANSFORMATEI DST IV AVÂND O COMPLEXITATE HARDWARE REDUSĂ

(Rezumat)

În această lucrare se prezintă un nou algoritm VLSI pentru implementarea hardware a transformatei DST IV avand o complexitate hardware redusă. Algoritmul VLSI propus a fost obținut printr-o restructurare adecvată a transformatei DST IV într-o singură structură computațională modulară şi regulată denumită band-correlation. Algoritmul propus poate fi mapat efficient pe o singură arie sistolică liniară având un număr redus de canale de intrare/ieşire cu o lățime de bandă redusă şi prezintă toate avantajele implementărilor VLSI folosind arii sistolice ce au la bază corelația circulară cum ar fi o topologie arhitecturală bună cu o structură de interconectare având legături scurte şi locale, un grad ridicat de regularitate şi modularitate şi viteză ridicată de procesare.